Features

- Ultra High Performance
  - System Speeds to 100 MHz
  - Array Multipliers > 50 MHz
  - 10 ns Flexible SRAM
  - Internal Tri-state Capability in Each Cell
- FreeRAM™
  - Flexible, Single/Dual Port, Synchronous/Asynchronous 10 ns SRAM
  - 2,048 - 18,432 Bits of Distributed SRAM Independent of Logic Cells
- 128 - 384 PCI Compliant I/Os
  - Programmable Output Drive
  - Fast, Flexible Array Access Facilitates Pin Locking
  - Pin-compatible with XC4000, XC5200 FPGAs
- 8 Global Clocks
  - Fast, Low Skew Clock Distribution
  - Programmable Rising/Falling Edge Transitions
  - Distributed Clock Shutdown Capability for Low Power Management
  - Global Reset/Asynchronous Reset Options
  - 4 Additional Dedicated PCI Clocks
- Cache Logic® Dynamic Full/Partial Re-configurability In-System
  - Unlimited Re-programmability via Serial or Parallel Modes
  - Enables Adaptive Designs
  - Enables Fast Vector Multiplier Updates
  - QuickChange™ Tools for Fast, Easy Design Changes
- Pin-compatible Package Options
  - Plastic Leaded Chip Carriers (PLCC)
  - Thin, Plastic Quad Flat Packs (LQFP, TQFP, PQFP)
  - Ball Grid Arrays (SBGA)
- Industry-standard Design Tools
  - Seamless Integration (Libraries, Interface, Full Back-annotation) with Concept®, Everest, Exemplar™, Mentor®, OrCAD®, Synario™, Synopsys®, Verilog®, Veribest®, Viewlogic®, Synplicity®
  - Timing Driven Placement & Routing
  - Automatic/Interactive Multi-chip Partitioning
  - Fast, Efficient Synthesis
  - Over 75 Automatic Component Generators Create 1000s of Reusable, Fully Deterministic Logic and RAM Functions
- Intellectual Property Cores
  - Fir Filters, UARTs, PCI, FFT and Other System Level Functions
- Easy Migration to Atmel Gate Arrays for High Volume Production
- Supply Voltage 3.3V
- 5V I/O Tolerant

5K - 50K Gates Coprocessor FPGA with FreeRAM™

AT40K05AL
AT40K10AL
AT40K20AL
AT40K40AL

Rev. 2818D–FPGA–02/03

Table 1. AT40KAL Family[1]

Device	AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL
Usable Gates	5K - 10K	10K - 20K	20K - 30K	40K - 50K
Rows x Columns	16 x 16	24 x 24	32 x 32	48 x 48
Cells	256	576	1,024	2,304
Registers	496[1]	954[1]	1,520[1]	3,048[1]
RAM Bits	2,048	4,608	8,192	18,432
I/O (Maximum)	128	192	256	384

Note: 1. Packages with FCK will have 8 less registers.

Description

The AT40KAL is a family of fully PCI-compliant, SRAM-based FPGAs with distributed 10 ns programmable synchronous/asynchronous, dual-port/single-port SRAM, 8 global clocks, Cache Logic ability (partially or fully reconfigurable without loss of data), automatic component generators, and range in size from 5,000 to 50,000 usable gates. I/O counts range from 128 to 384 in industry standard packages ranging from 84-pin PLCC to 352-ball Square BGA, and support 3.3V designs.

The AT40KAL is designed to quickly implement high-performance, large gate count designs through the use of synthesis and schematic-based tools used on a PC or Sun platform. Atmel's design tools provide seamless integration with industry standard tools such as Synplicity, ModelSim, Exemplar and Viewlogic. See the "IDS Datasheet" available on the Atmel web site (http://www.atmel.com/atmel/acrobat/doc1421.pdf) for a list of other supported tools.

The AT40KAL can be used as a coprocessor for high-speed (DSP/processor-based) designs by implementing a variety of computation intensive, arithmetic functions. These include adaptive finite impulse response (FIR) filters, fast Fourier transforms (FFT), convolvers, interpolators and discrete-cosine transforms (DCT) that are required for video compression and decompression, encryption, convolution and other multimedia applications.

Fast, Flexible and Efficient SRAM

The AT40KAL FPGA offers a patented distributed 10 ns SRAM capability where the RAM can be used without losing logic resources. Multiple independent, synchronous or asynchronous, dual-port or single-port RAM functions (FIFO, scratch pad, etc.) can be created using Atmel's macro generator tool.

Fast, Efficient Array and Vector Multipliers

The AT40KAL's patented 8-sided core cell with direct horizontal, vertical and diagonal cell-to-cell connections implements ultra fast array multipliers without using any busing resources. The AT40KAL's Cache Logic capability enables a large number of design coefficients and variables to be implemented in a very small amount of silicon, enabling vast improvement in system speed at much lower cost than conventional FPGAs.

Cache Logic Design

The AT40KAL, AT6000 and FPSLIC families are capable of implementing Cache Logic (dynamic full/partial logic reconfiguration, without loss of data, on-the-fly) for building adaptive logic and systems. As new logic functions are required, they can be loaded into the logic cache without losing the data already there or disrupting the operation of the rest of the chip; replacing or complementing the active logic. The AT40KAL can act as a reconfigurable coprocessor.

Automatic Component Generators

The AT40KAL FPGA family is capable of implementing user-defined, automatically generated, macros in multiple designs; speed and functionality are unaffected by the macro orientation or density of the target device. This enables the fastest, most predictable and efficient FPGA design approach and minimizes design risk by reusing already proven functions. The Automatic Component Generators work seamlessly with industry standard schematic and synthesis tools to create the fastest, most efficient designs available.

The patented AT40KAL series architecture employs a symmetrical grid of small yet powerful cells connected to a flexible busing network. Independently controlled clocks and resets govern every column of cells. The array is surrounded by programmable I/O.

Devices range in size from 5,000 to 50,000 usable gates in the family, and have 256 to 3,048 registers. Pin locations are consistent throughout the AT40KAL series for easy design migration in the same package footprint. The AT40KAL series FPGAs utilize a reliable 0.35µ triple-metal, CMOS process and are 100% factory-tested. Atmel's PC- and workstation-based integrated development system (IDS) is used to create AT40KAL series designs. Multiple design entry methods are supported.

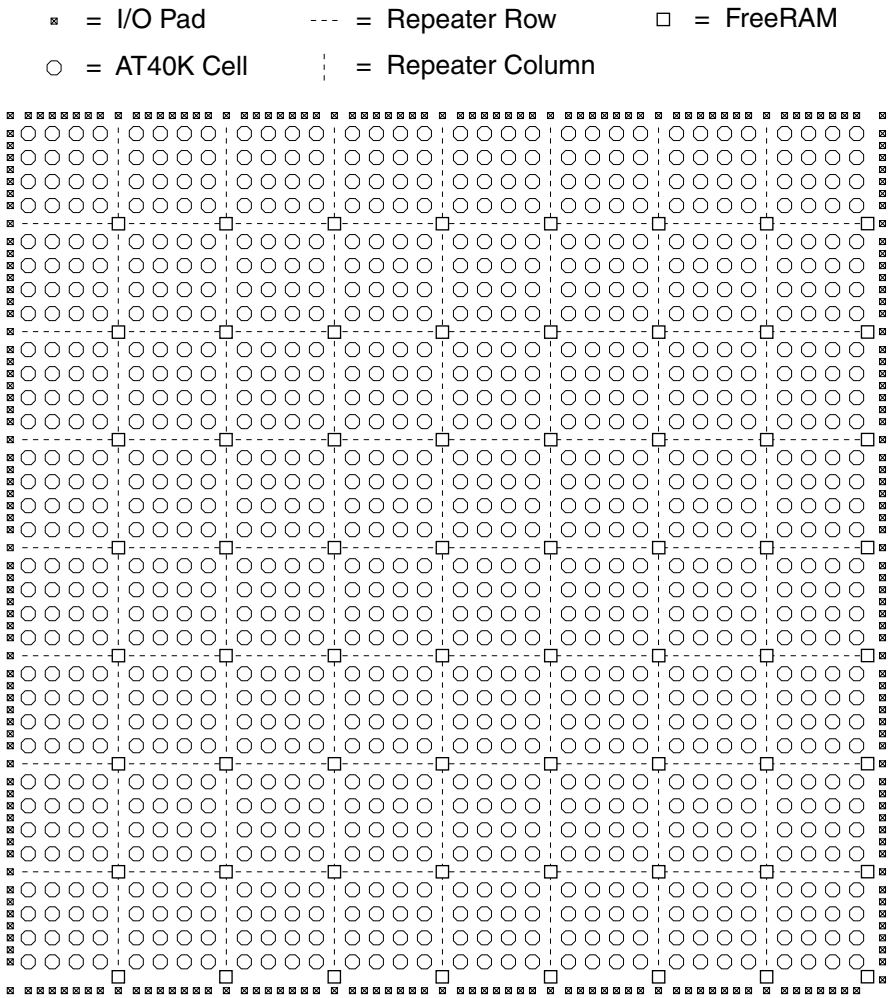
The Atmel architecture was developed to provide the highest levels of performance, functional density and design flexibility in an FPGA. The cells in the Atmel array are small, efficient and can implement any pair of Boolean functions of (the same) three inputs or any single Boolean function of four inputs. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances.

The Symmetrical Array

At the heart of the Atmel architecture is a symmetrical array of identical cells, see Figure 1. The array is continuous from one edge to the other, except for bus repeaters spaced every four cells, see Figure 2 on page 5. At the intersection of each repeater row and column there is a 32 x 4 RAM block accessible by adjacent buses. The RAM can be configured as either a single-ported or dual-ported RAM(1), with either synchronous or asynchronous operation.

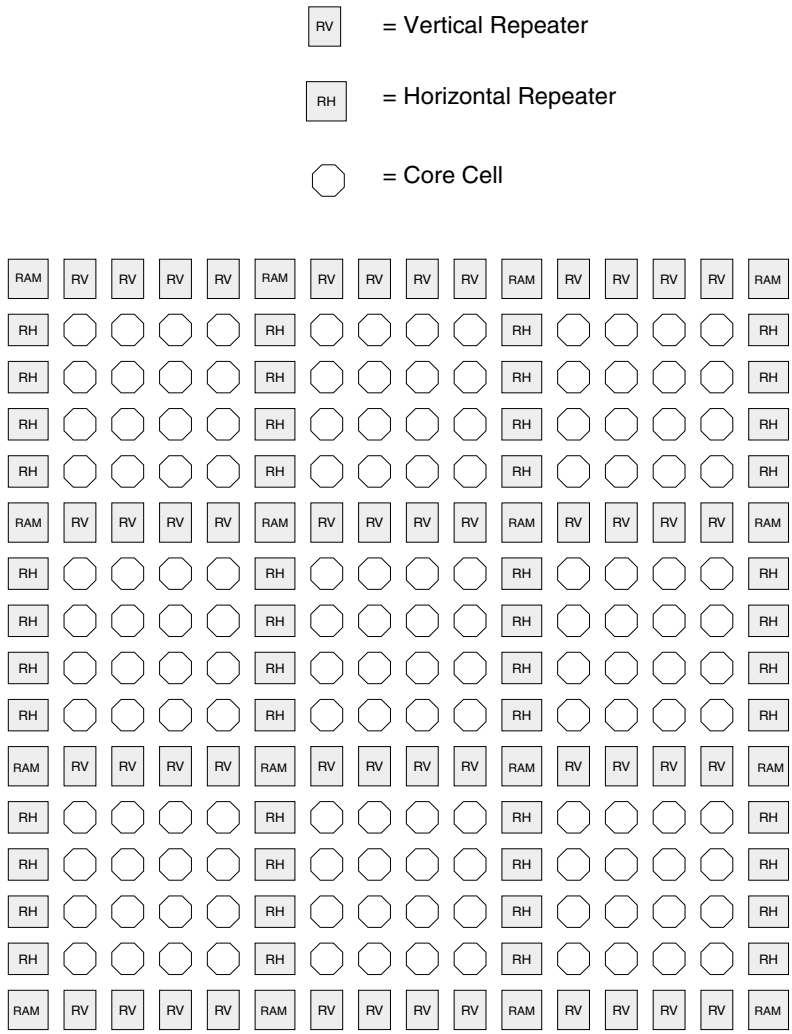
Note: 1. The right-most column can only be used as single-port RAM.

Figure 1. Symmetrical Array Surrounded by I/O (AT40K20AL)(1)



Note: 1. AT40KAL has registered I/Os. Group enable on every sector for tri-states on obufe's.

Figure 2. Floor Plan (Representative Portion)[1]



Note: 1. Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane. Each repeater has connections to two adjacent local-bus segments and two express-bus segments. This is done automatically using the integrated development system (IDS) tool.

The Busing Network

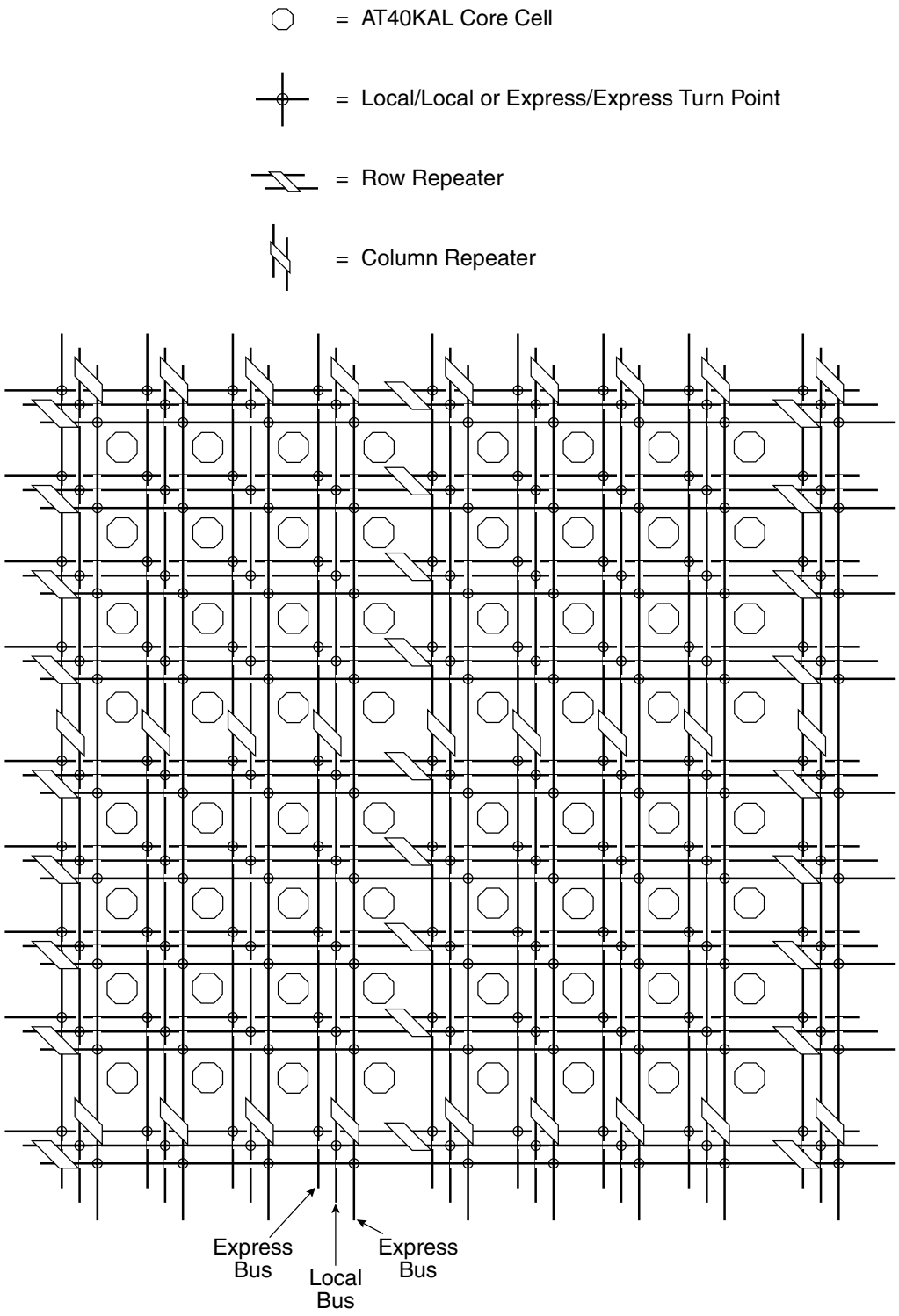
Figure 3 on page 7 depicts one of five identical busing planes. Each plane has three bus resources: a local-bus resource (the middle bus) and two express-bus (both sides) resources. Bus resources are connected via repeaters. Each repeater has connections to two adjacent local-bus segments and two express-bus segments. Each local-bus segment spans four cells and connects to consecutive repeaters. Each express-bus segment spans eight cells and "leapfrogs" or bypasses a repeater. Repeaters regenerate signals and can connect any bus to any other bus (all pathways are legal) on the same plane. Although not shown, a local bus can bypass a repeater via a programmable pass gate allowing long on-chip tri-state buses to be created. Local/Local turns are implemented through pass gates in the cell-bus interface. Express/Express turns are implemented through separate pass gates distributed throughout the array.

Some of the bus resources on the AT40KAL are used as a dual-function resources. Table 2 shows which buses are used in a dual-function mode and which bus plane is used. The AT40KAL software tools are designed to accommodate dual-function buses in an efficient manner.

Table 2. Dual-function Buses

Function	Type	Plane(s)	Direction	Comments
Cell Output Enable	Local	5	Horizontal and Vertical	
RAM Output Enable	Express	2	Vertical	Bus full length at array edge Bus in first column to left of RAM block
RAM Write Enable	Express	1	Vertical	Bus full length at array edge Bus in first column to left of RAM block
RAM Address	Express	1 - 5	Vertical	Buses full length at array edge Buses in second column to left of RAM block
RAM Data In	Local	1	Horizontal	Data In connects to local bus plane 1
RAM Data Out	Local	2	Horizontal	Data out connects to local bus plane 2
Clocking	Express	4	Vertical	Bus half length at array edge
Set/Reset	Express	5	Vertical	Bus half length at array edge

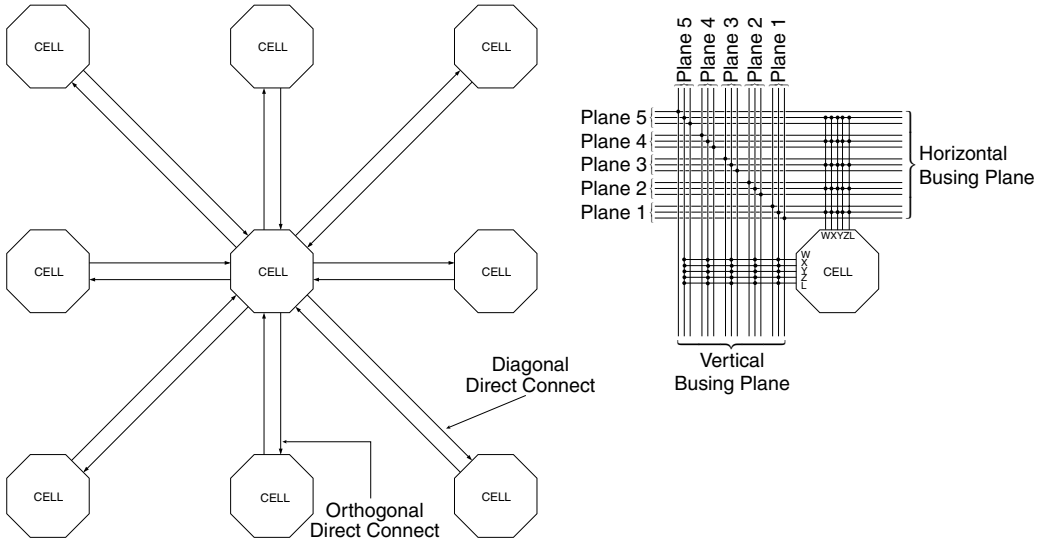
Figure 3. Busing Plane (One of Five)



Cell Connections

Figure 4(a) depicts direct connections between a cell and its eight nearest neighbors. Figure 4(b) shows the connections between a cell and five horizontal local buses (1 per busing plane) and five vertical local buses (1 per busing plane).

Figure 4. Cell Connections



(a) Cell-to-cell Connections

(b) Cell-to-bus Connections

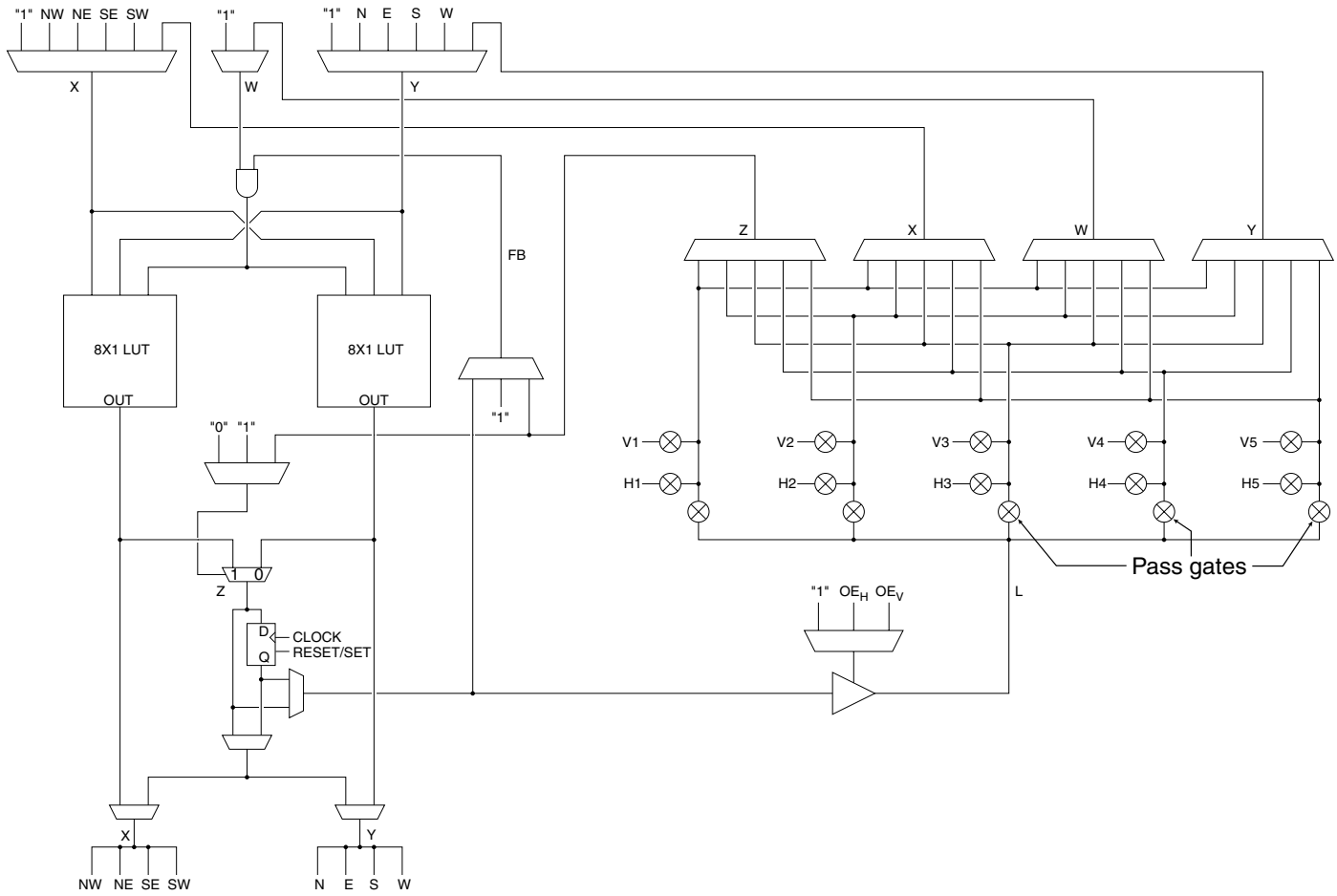
The Cell

Figure 5 depicts the AT40KAL cell. Configuration bits for separate muxes and pass gates are independent. All permutations of programmable muxes and pass gates are legal. V_n (V_1 - V_5) is connected to the vertical local bus in plane n. H_n (H_1 - H_5) is connected to the horizontal local bus in plane *n*. A local/local turn in plane n is achieved by turning on the two pass gates connected to V_n and H_n. Pass gates are opened to let signals into the cell from a local bus or to drive a signal out onto a local bus. Signals coming into the logic cell on one local bus plane can be switched onto another plane by opening two of the pass gates. This allows bus signals to switch planes to achieve greater route ability. Up to five simultaneous local/local turns are possible.

The AT40KAL FPGA core cell is a highly configurable logic block based around two 3-input LUTs (8 x 1 ROM), which can be combined to produce one 4-input LUT. This means that any core cell can implement two functions of 3 inputs or one function of 4 inputs. There is a Set/Reset D flip-flop in every cell, the output of which may be tri-stated and fed back internally within the core cell. There is also a 2-to-1 multiplexer in every cell, and an upstream AND gate in the “front end” of the cell. This AND gate is an important feature in the implementation of efficient array multipliers.

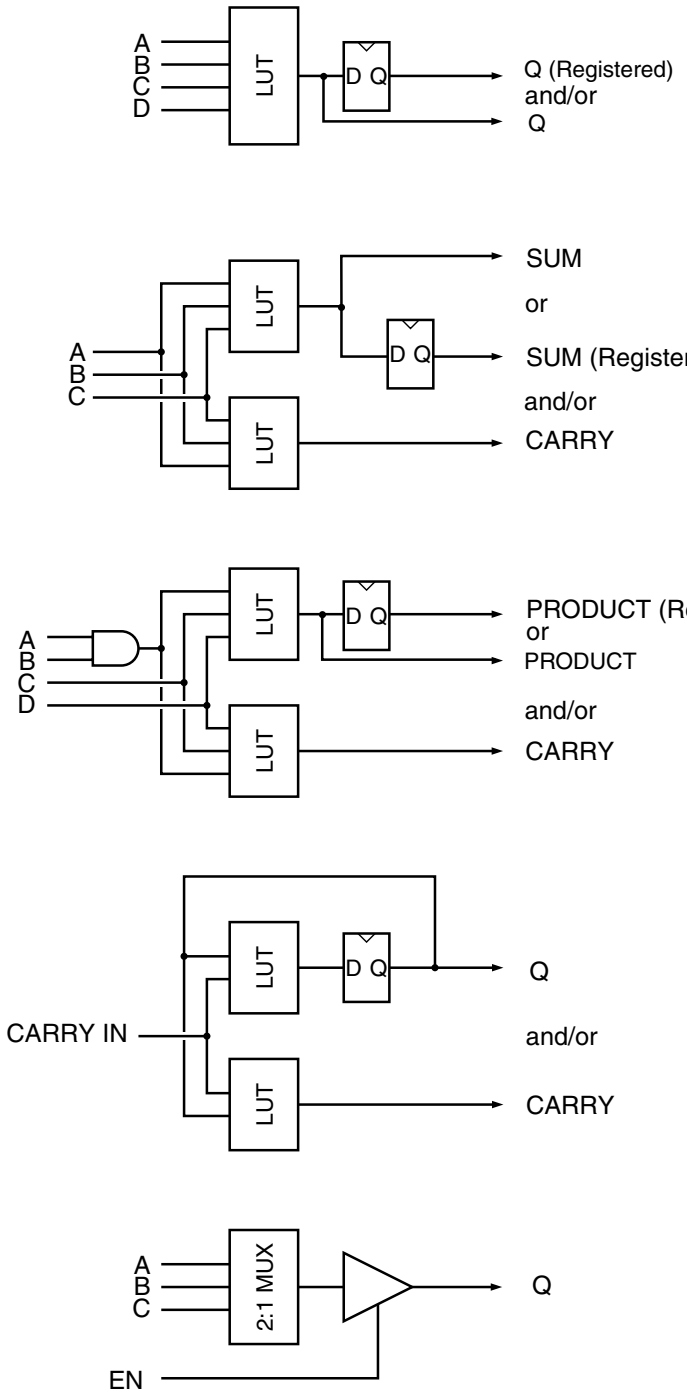
With this functionality in each core cell, the core cell can be configured in several “modes”. The core cell flexibility makes the AT40KAL architecture well suited to most digital design application areas, see Figure 6.

Figure 5. The Cell



X = Diagonal Direct Connect or Bus
Y = Orthogonal Direct Connect or Bus
W = Bus Connection
Z = Bus Connection
FB = Internal Feedback

Figure 6. Some Single Cell Modes



Synthesis Mode. This mode is particularly important for the use of VHDL/Verilog design. VHDL/Verilog Synthesis tools generally will produce as their output large amounts of random logic functions. Having a 4-input LUT structure gives efficient random logic optimization without the delays associated with larger LUT structures. The output of any cell may be registered, tri-stated and/or fed back into a core cell.

Arithmetic Mode is frequently used in many designs. As can be seen in the figure, the AT40KAL core cell can implement a 1-bit full adder (2-input adder with both Carry In and Carry Out) in one core cell. Note that the sum output in this diagram is registered. This output could then be tri-stated and/or fed back into the cell.

DSP/Multiplier Mode. This mode is used to efficiently implement array multipliers. An array multiplier is an array of bitwise multipliers, each implemented as a full adder with an upstream AND gate. Using this AND gate and the diagonal interconnects between cells, the array multiplier structure fits very well into the AT40KAL architecture.

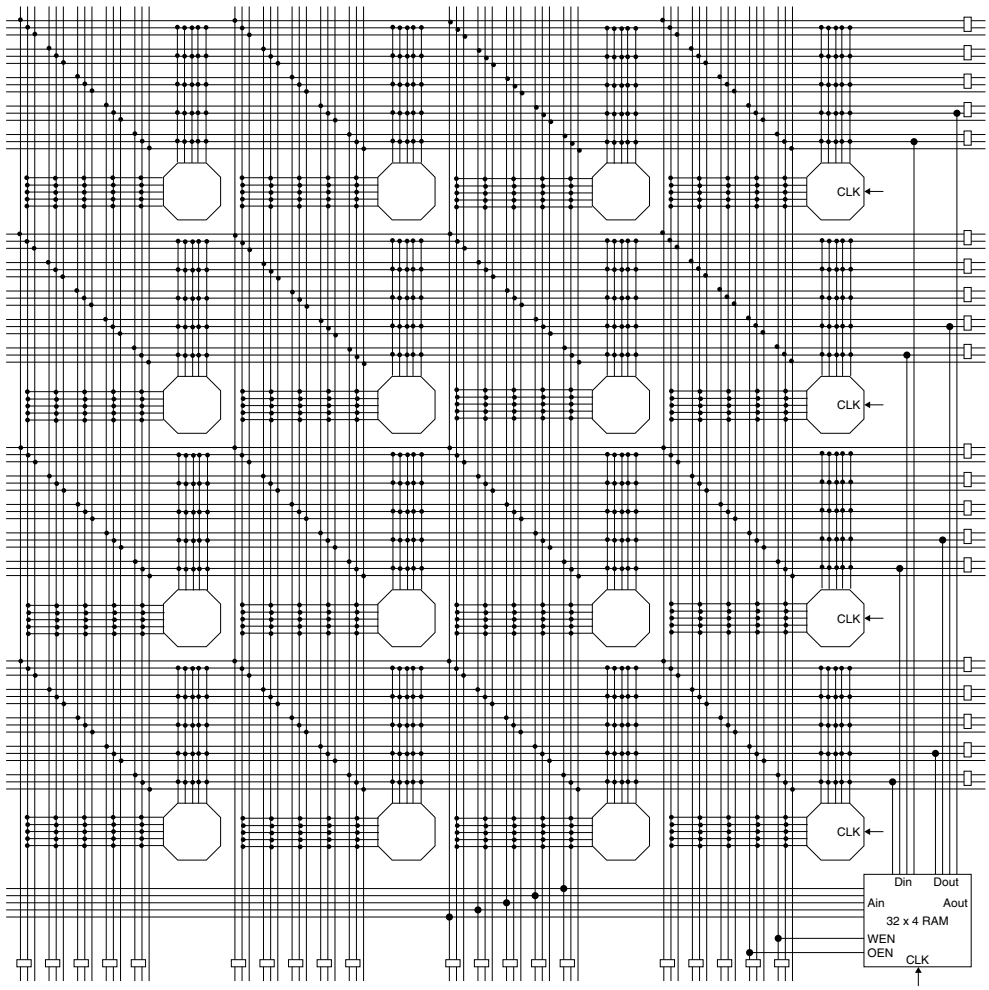
Counter Mode. Counters are fundamental to almost all digital designs. They are the basis of state machines, timing chains and clock dividers. A counter is essentially an increment by one function (i.e., an adder), with the input being an output (or a decode of an output) from the previous stage. A 1-bit counter can be implemented in one core cell. Again, the output can be registered, tri-stated and/or fed back.

Tri-state/Mux Mode. This mode is used in many telecommunications applications, where data needs to be routed through more than one possible path. The output of the core cell is very often tri-statable for many inputs to many outputs data switching.

RAM

32 x 4 dual-ported RAM blocks are dispersed throughout the array, see Figure 7. A 4-bit Input Data Bus connects to four horizontal local buses distributed over four sector rows (plane 1). A 4-bit Output Data Bus connects to four horizontal local buses distributed over four sector rows (plane 2). A 5-bit Input Address Bus connects to five vertical express buses in the same column. A 5-bit Output Address Bus connects to five vertical express buses in the same column. Ain (input address) and Aout (output address) alternate positions in horizontally aligned RAM blocks. For the left-most RAM blocks, Aout is on the left and Ain is on the right. For the right-most RAM blocks, Ain is on the left and Aout is tied off, thus it can only be configured as a single port. For single-ported RAM, Ain is the READ/WRITE address port and Din is the (bi-directional) data port. Right-most RAM blocks can be used only for single-ported memories. WEN and OEN connect to the vertical express buses in the same column.

Figure 7. RAM Connections (One Ram Block)



Reading and writing of the 10 ns 32 x 4 dual-port FreeRAM are independent of each other. Reading the 32 x 4 dual-port RAM is completely asynchronous. Latches are transparent; when Load is logic 1, data flows through; when Load is logic 0, data is latched. These latches are used to synchronize Write Address, $\overline{\text{Write Enable Not}}$, and Din signals for a synchronous RAM. Each bit in the 32 x 4 dual-port RAM is also a transparent latch. The front-end latch and the memory latch together form an edge-triggered flip flop. When a nibble (bit = 7) is (Write) addressed and LOAD is logic 1 and $\overline{\text{WE}}$ is logic 0, data flows through the bit. When a nibble is not (Write) addressed or LOAD is logic 0 or $\overline{\text{WE}}$ is logic 1, data is latched in the nibble. The two CLOCK muxes are controlled together; they both select CLOCK (for a synchronous RAM) or they both select "1" (for an asynchronous RAM). CLOCK is obtained from the clock for the sector-column immediately to the left and immediately above the RAM block. Writing any value to the RAM clear byte during configuration clears the RAM (see the "AT40K/40KAL Configuration Series" application note at www.atmel.com).

Figure 8. RAM Logic

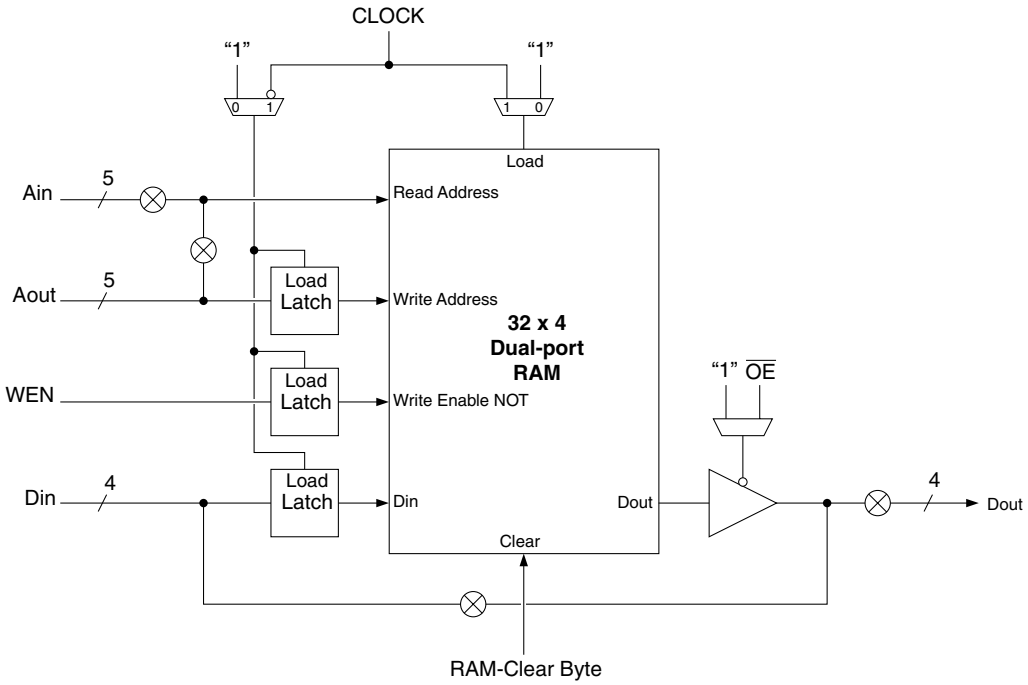
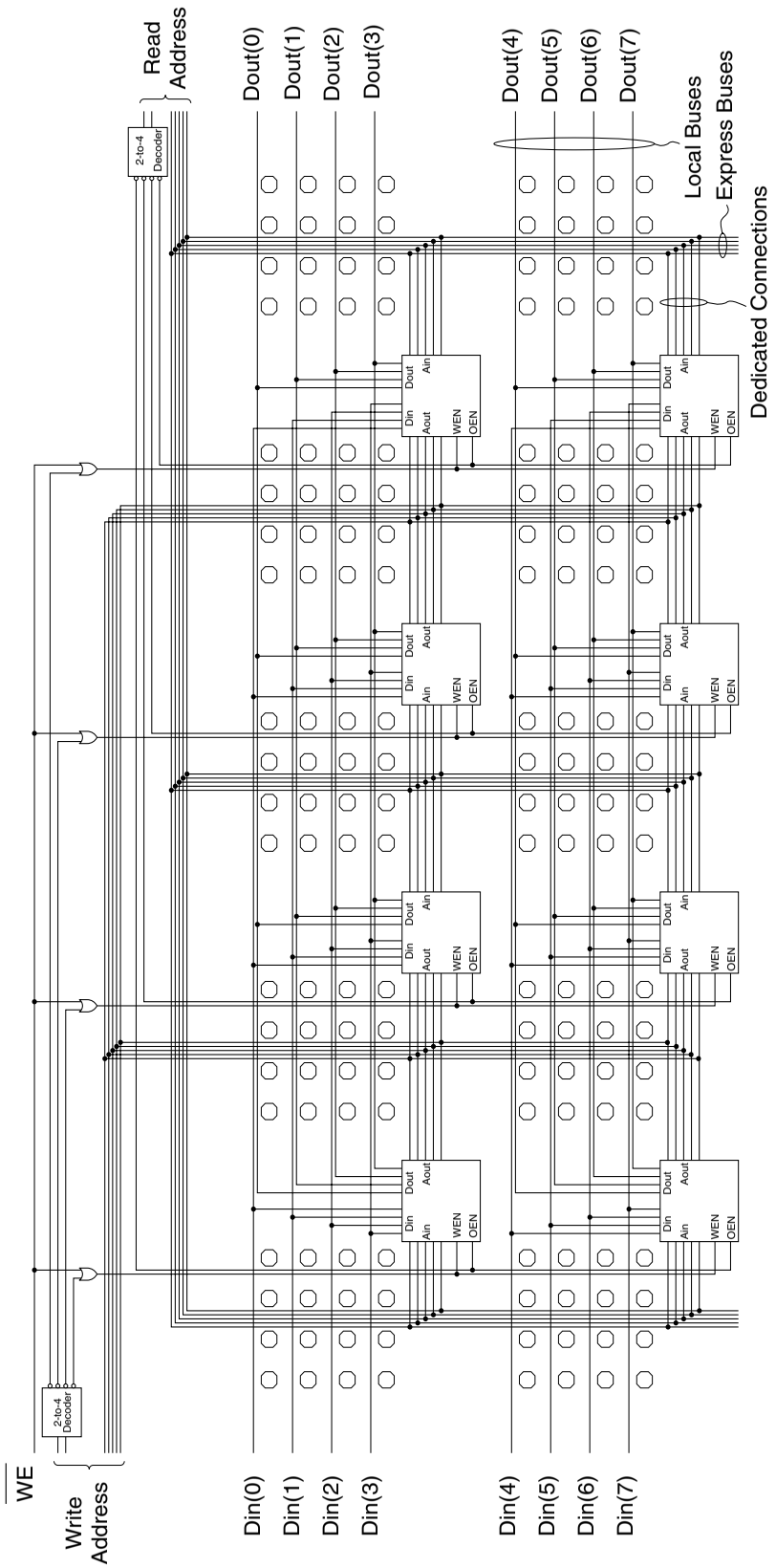


Figure 9 on page 13 shows an example of a RAM macro constructed using the AT40KAL's FreeRAM cells. The macro shown is a 128 x 8 dual-ported asynchronous RAM. Note the very small amount of external logic required to complete the address decoding for the macro. Most of the logic cells (core cells) in the sectors occupied by the RAM will be unused: they can be used for other logic in the design. This logic can be automatically generated using the macro generators.

Figure 9. RAM Example: 128 x 8 Dual-ported RAM (Asynchronous)



Clocking Scheme

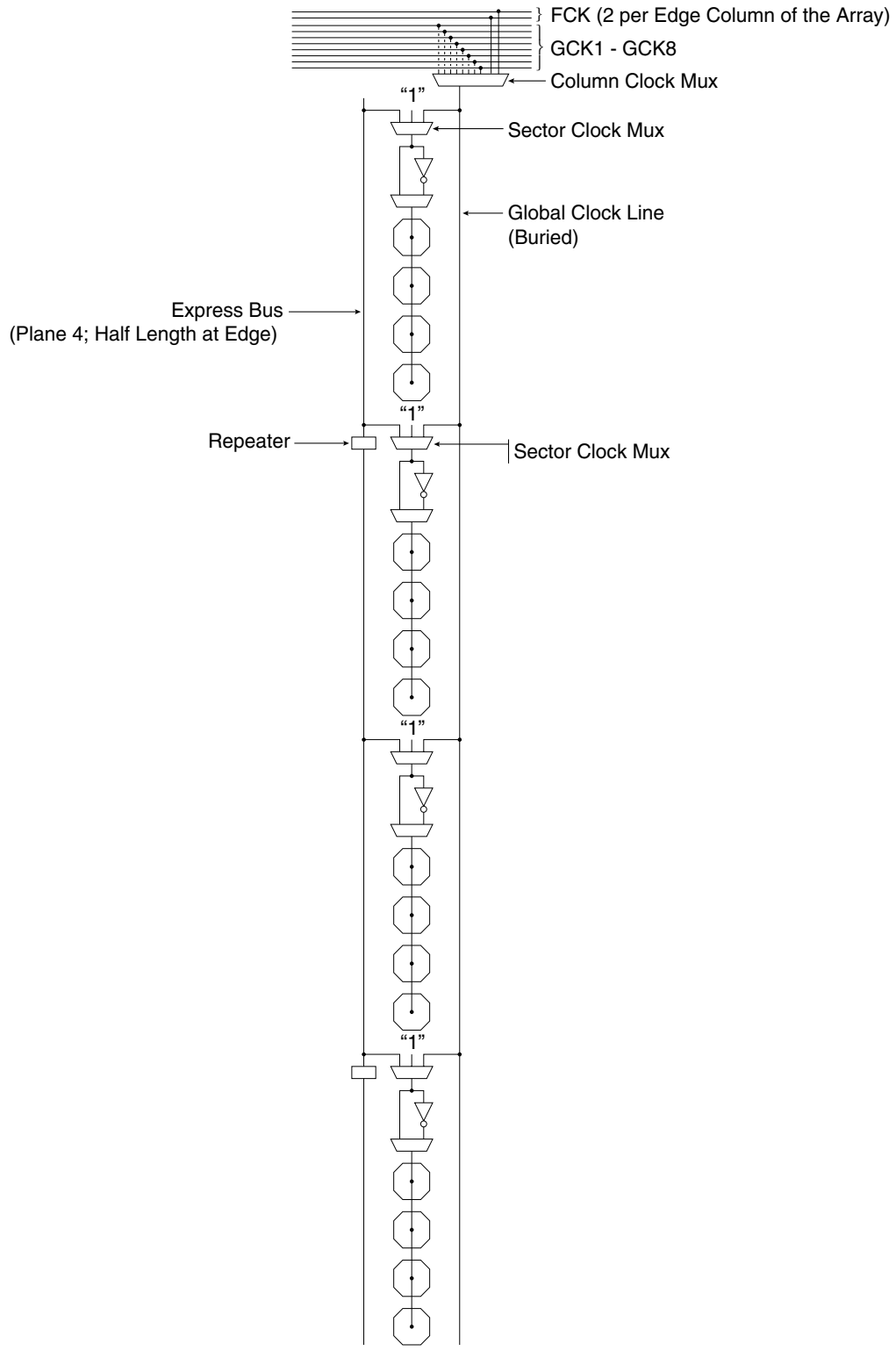
There are eight Global Clock buses (GCK1 - GCK8) on the AT40KAL FPGA. Each of the eight dedicated Global Clock buses is connected to one of the dual-use Global Clock pins. Any clocks used in the design should use global clocks where possible: this can be done by using Assign Pin Locks to lock the clocks to the Global Clock locations. In addition to the eight Global Clocks, there are four Fast Clocks (FCK1 - FCK4), two per edge column of the array for PCI specification. For AT40KAL FPGAs, even the derived clocks can be routed through the Global network. Access points are provided in the corners of the array to route the derived clocks into the global clock network. The IDS software tools handle derived clocks to global clock connections automatically if used.

Each column of an array has a “Column Clock mux” and a “Sector Clock mux”. The Column Clock mux is at the top of every column of an array and the Sector Clock mux is at every four cells. The Column Clock mux is selected from one of the eight Global Clock buses. The clock provided to each sector column of four cells is inverted, non-inverted or tied off to “0”, using the Sector Clock mux to minimize the power consumption in a sector that has no clocks. The clock can either come from the Column Clock or from the Plane 4 express bus, see Figure 10 on page 15. The extreme-left Column Clock mux has two additional inputs, FCK1 and FCK2, to provide fast clocking to left-side I/Os. The extreme-right Column Clock mux has two additional inputs as well, FCK3 and FCK4, to provide fast clocking to right-side I/Os.

The register in each cell is triggered on a rising clock edge by default. Before configuration on power-up, constant “0” is provided to each register’s clock pins. After configuration on power-up, the registers either set or reset, depending on the user’s choice.

The clocking scheme is designed to allow efficient use of multiple clocks with low clock skew, both within a column and across the core cell array.

Figure 10. Clocking (for One Column of Cells)



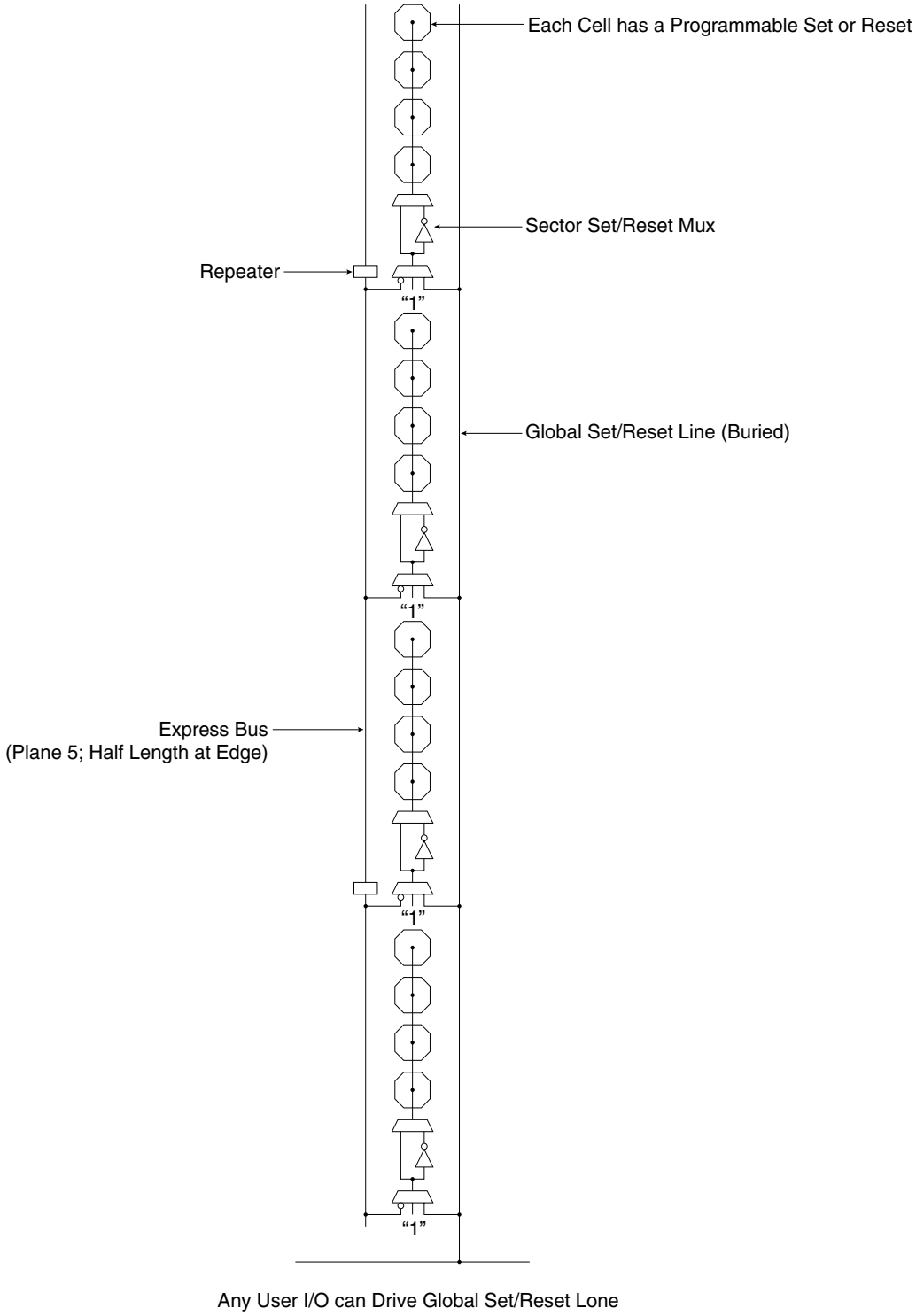
Set/Reset Scheme

The AT40KAL family reset scheme is essentially the same as the clock scheme except that there is only one Global Reset. A dedicated Global Set/Reset bus can be driven by any User I/O, except those used for clocking (Global Clocks or Fast Clocks). The automatic placement tool will choose the reset net with the most connections to use the global resources. You can change this by using an RSBUF component in your design to indicate the global reset. Additional resets will use the express bus network.

The Global Set/Reset is distributed to each column of the array. Like Sector Clock mux, there is Sector Set/Reset mux at every four cells. Each sector column of four cells is set/reset by a Plane 5 express bus or Global Set/Reset using the Sector Set/Reset mux, see Figure 11 on page 17. The set/reset provided to each sector column of four cells is either inverted or non-inverted using the Sector Reset mux.

The function of the Set/Reset input of a register is determined by a configuration bit in each cell. The Set/Reset input of a register is active low (logic 0) by default. Setting or Resetting of a register is asynchronous. Before configuration on power-up, a logic 1 (a high) is provided by each register (i.e., all registers are set at power-up).

Figure 11. Set/Reset (for One Column of Cells)



I/O Structure

The AT40KAL has registered I/Os and group enable every sector for tri-states on obuf's.

PAD

The I/O pad is the one that connects the I/O to the outside world. Note that not all I/Os have pads: the ones without pads are called Unbonded I/Os. The number of unbonded I/Os varies with the device size and package. These unbonded I/Os are used to perform a variety of bus turns at the edge of the array.

PULL-UP/PULL-DOWN

Each pad has a programmable pull-up and pull-down attached to it. This supplies a weak "1" or "0" level to the pad pin. When all other drivers are off, this control will dictate the signal level of the pad pin.

The input stage of each I/O cell has a number of parameters that can be programmed either as properties in schematic entry or in the I/O Pad Attributes editor in IDS.

CMOS

The threshold level is a CMOS-compatible level.

SCHMITT

A Schmitt trigger circuit can be enabled on the inputs. The Schmitt trigger is a regenerative comparator circuit that adds 1V hysteresis to the input. This effectively improves the rise and fall times (leading and trailing edges) of the incoming signal and can be useful for filtering out noise.

DELAYS

The input buffer can be programmed to include four different intrinsic delays as specified in the AC timing characteristics. This feature is useful for meeting data hold requirements for the input signal.

DRIVE

The output drive capabilities of each I/O are programmable. They can be set to FAST, MEDIUM or SLOW (using IDS tool). The FAST setting has the highest drive capability (20 mA at 5V) buffer and the fastest slew rate. MEDIUM produces a medium drive (14 mA at 5V) buffer, while SLOW yields a standard (6 mA at 5V) buffer.

TRI-STATE

The output of each I/O can be made tri-state (0, 1 or Z), open source (1 or Z) or open drain (0 or Z) by programming an I/O's Source Selection mux. Of course, the output can be normal (0 or 1), as well.

SOURCE SELECTION MUX

The Source Selection mux selects the source for the output signal of an I/O.

Primary, Secondary and Corner I/Os

The AT40KAL has three kinds of I/Os: Primary I/O, Secondary I/O and a Corner I/O. Every edge cell except corner cells on the AT40KAL has access to one Primary I/O and two Secondary I/Os.

Primary I/O

Every logic cell at the edge of the FPGA array has a direct orthogonal connection to and from a Primary I/O cell. The Primary I/O interfaces directly to its adjacent core cell. It also connects into the repeaters on the row immediately above and below the adjacent core cell. In addition, each Primary I/O also connects into the busing network of the three nearest edge cells. This is an extremely powerful feature, as it provides logic cells toward the center of the array with fast access to I/Os via local and express buses. It can be seen from the diagram that a given Primary I/O can be accessed from any logic cell on three separate rows or columns of the FPGA. See Figure 12 on page 20.

Secondary I/O

Every logic cell at the edge of the FPGA array has two direct diagonal connections to a Secondary I/O cell. The Secondary I/O is located between core cell locations. This I/O connects on the diagonal inputs to the cell above and the cell below. It also connects to the repeater of the cell above and below. In addition, each Secondary I/O also connects into the busing network of the two nearest edge cells. This is an extremely powerful feature, as it provides logic cells toward the center of the array with fast access to I/Os via local and express buses. It can be seen from the diagram that a given Secondary I/O can be accessed from any logic cell on two rows or columns of the FPGA. See Figure 13 on page 20.

Corner I/O

Logic cells at the corner of the FPGA array have direct-connect access to five separate I/Os: 2 Primary, 2 Secondary and 1 Corner I/O. Corner I/Os are like an extra Secondary I/O at each corner of the array. With the inclusion of Corner I/Os, an AT40KAL FPGA with n x n core cells always has 8n I/Os. As the diagram shows, Corner I/Os can be accessed both from the corner logic cell and the horizontal and vertical busing networks running along the edges of the array. This means that many different edge logic cells can access the Corner I/Os. See Figure 14 on page 21.

Figure 12. West Primary I/O (Mirrored for East I/O)

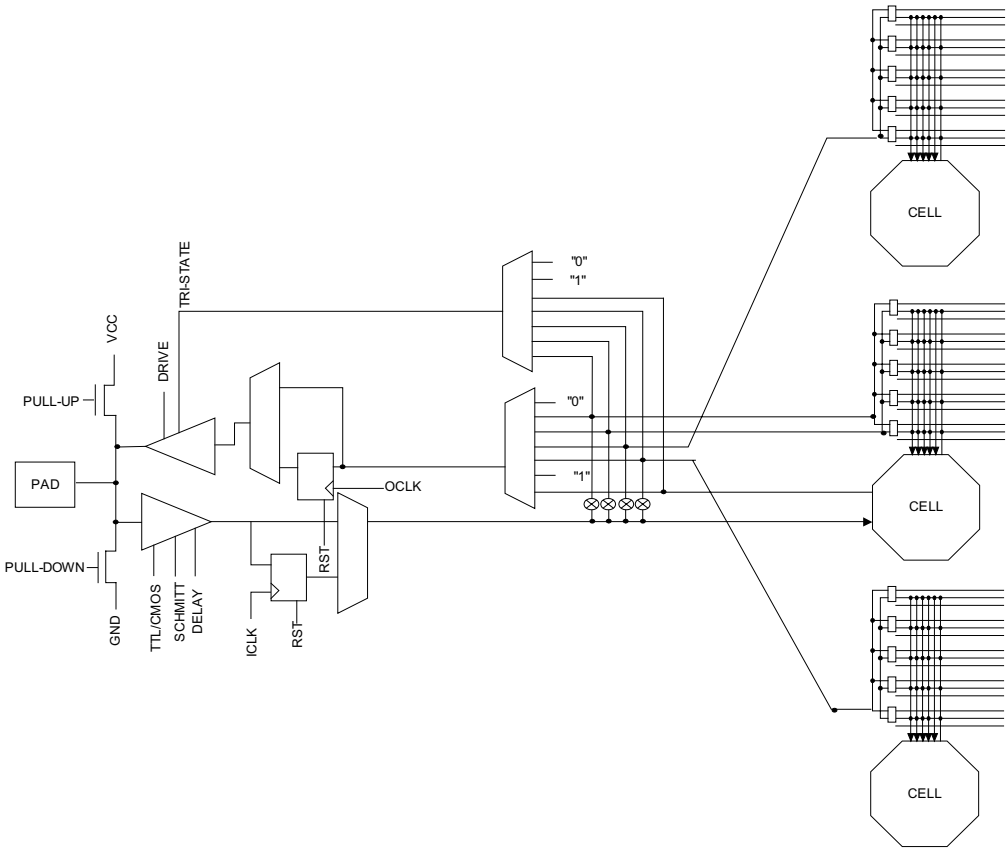


Figure 13. West Secondary I/O (Mirrored for East I/O)

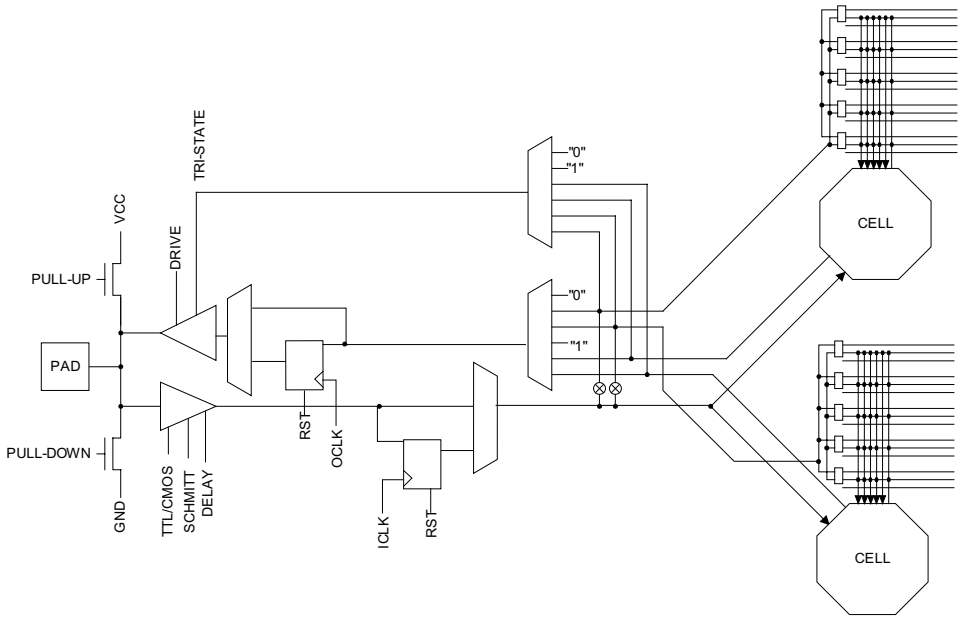
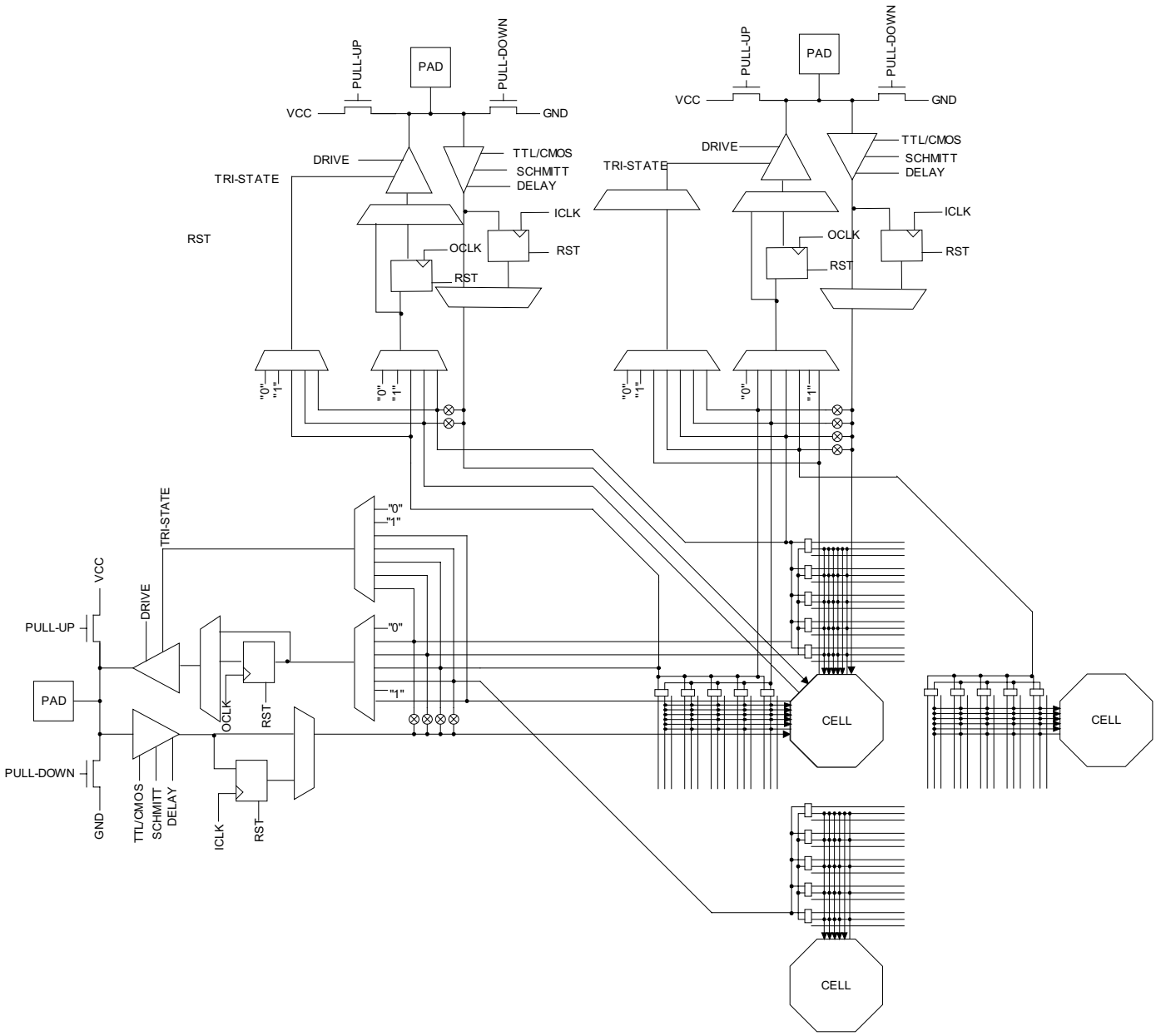


Figure 14. Northwest Corner I/O (Similar NE/SE/SW Corners)



Absolute Maximum Ratings – 3.3V Commercial/Industrial*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.5V to V_{CC} +7V
Supply Voltage (V_{CC})	-0.5V to +7.0V
Maximum Soldering Temp. (10 sec. @ 1/16 in.)	250°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

DC and AC Operating Range – 3.3V Operation

		Commercial	Industrial
Operating Temperature (Case)		0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply		3.3V ± 0.3V	3.3V ± 0.3V
Input Voltage Level (CMOS)	High (V_{IHC})	70% - 100% V_{CC}	70% - 100% V_{CC}
	Low (V_{ILC})	0 - 30% V_{CC}	0 - 30% V_{CC}

DC Characteristics – 3.3V Operation Commercial/Industrial

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IH}	High-level Input Voltage	CMOS	0.7 V_{CC}		5.5V	V
V_{IL}	Low-level Input Voltage	CMOS	-0.3		30% V_{CC}	V
V_{OH}	High-level Output Voltage	I_{OH} = 4 mA V_{CC} = V_{CC} minimum	2.1			V
		I_{OH} = 12 mA V_{CC} = 3.0V	2.1			V
		I_{OH} = 16 mA V_{CC} = 3.0V	2.1			V
V_{OL}	Low-level Output Voltage	I_{OL} = -4 mA V_{CC} = 3.0V			0.4	V
		I_{OL} = -12 mA V_{CC} = 3.0V			0.4	V
		I_{OL} = -16 mA V_{CC} = 3.0V			0.4	V
I_{IH}	High-level Input Current	V_{IN} = V_{CC} Maximum			10.0	µA
		With pull-down, V_{IN} = V_{CC}	75.0	150.0	300.0	µA
I_{IL}	Low-level Input Current	V_{IN} = V_{SS}	-10.0			µA
		With pull-up, V_{IN} = V_{SS}	-300.0	-150.0	-75.0	µA
I_{OZH}	High-level Tri-state Output Leakage Current	Without pull-down, V_{IN} = V_{CC} Maximum			10.0	µA
		With pull-down, V_{IN} = V_{CC} Maximum	75.0	150.0	300.0	µA
I_{OZL}	Low-level Tri-state Output Leakage Current	Without pull-up, V_{IN} = V_{SS}	-10.0			mA
		With pull-up, V_{IN} = V_{SS}	CON = -500 µA TO -125 µA	-150.0	CON = -500 µA TO -125 µA	µA
I_{CC}	Standby Current Consumption	Standby, unprogrammed		0.6	1.0	mA
C_{IN}	Input Capacitance	All pins			10.0	pF

Note: 1. Parameter based on characterization and simulation; it is not tested in production.

Power-On Power Supply Requirements

Atmel FPGAs require a minimum rated power supply current capacity to insure proper initialization, and the power supply ramp-up time does affect the current required. A fast ramp-up time requires more current than a slow ramp-up time.

Table 3. Power-On Power Supply Requirements[1]

Device	Description	Maximum Current[2][3]
AT40K05AL AT40K10AL	Maximum Current Supply	50 mA
AT40K20AL AT40K40AL	Maximum Current Supply	100 mA

Notes:
1. This specification applies to Commercial and Industrial grade products only.
2. Devices are guaranteed to initialize properly at 50% of the minimum current listed above. A larger capacity power supply may result in a larger initialization current.
3. Ramp-up time is measured from 0 V DC to 3.6 V DC. Peak current required lasts less than 2 ms, and occurs near the internal power on reset threshold voltage.

AC Timing Characteristics – 3.3V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.00V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.60V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

Cell Function	Parameter	Path	-1	Units	Notes
Core					
2-input Gate	t_{PD} (Maximum)	x/y -> x/y	1.8	ns	1 unit load
3-input Gate	t_{PD} (Maximum)	x/y/z -> x/y	2.1	ns	1 unit load
3-input Gate	t_{PD} (Maximum)	x/y/w -> x/y	2.2	ns	1 unit load
4-input Gate	t_{PD} (Maximum)	x/y/w/z -> x/y	2.2	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	y -> y	1.4	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	x -> y	1.7	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	y -> x	1.8	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	x -> x	1.5	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	w -> y	2.2	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	w -> x	2.3	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	z -> y	2.3	ns	1 unit load
Fast Carry	t_{PD} (Maximum)	z -> x	1.7	ns	1 unit load
DFF	t_{PD} (Maximum)	q -> x/y	1.8	ns	1 unit load
DFF	t_{PD} (Maximum)	R -> x/y	2.2	ns	1 unit load
DFF	t_{PD} (Maximum)	S -> x/y	2.2	ns	1 unit load
DFF	t_{PD} (Maximum)	q -> w	1.8	ns	
Incremental -> L	t_{PD} (Maximum)	x/y -> L	1.5	ns	1 unit load
Local Output Enable	t_{PZX} (Maximum)	oe -> L	1.4	ns	1 unit load
Local Output Enable	t_{PXZ} (Maximum)	oe -> L	1.8	ns	

AC Timing Characteristics – 3.3V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{DD}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD}.

Cell Function	Parameter	Path	-1	Units	Notes
Repeaters					
Repeater	t_{PD} (Maximum)	L -> E	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	E -> E	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	L -> L	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	E -> L	1.3	ns	1 unit load
Repeater	t_{PD} (Maximum)	E -> IO	0.8	ns	1 unit load
Repeater	t_{PD} (Maximum)	L -> IO	0.8	ns	1 unit load

All input IO characteristics measured from a V_{IH} of 50% of V_{DD} at the pad (CMOS threshold) to the internal V_{IH} of 50% of V_{DD}. All output IO characteristics are measured as the average of t_{PDLH} and t_{PDHL} to the pad V_{IH} of 50% of V_{DD}.

Cell Function	Parameter	Path	-1	Units	Notes
IO					
Input	t_{PD} (Maximum)	pad -> x/y	1.2	ns	No extra delay
Input	t_{PD} (Maximum)	pad -> x/y	3.6	ns	1 extra delay
Input	t_{PD} (Maximum)	pad -> x/y	7.3	ns	2 extra delays
Input	t_{PD} (Maximum)	pad -> x/y	10.8	ns	3 extra delays
Output, Slow	t_{PD} (Maximum)	x/y/E/L -> pad	5.9	ns	50 pf load
Output, Medium	t_{PD} (Maximum)	x/y/E/L -> pad	4.8	ns	50 pf load
Output, Fast	t_{PD} (Maximum)	x/y/E/L -> pad	3.9	ns	50 pf load
Output, Slow	t_{PZX} (Maximum)	oe -> pad	6.2	ns	50 pf load
Output, Slow	t_{PXZ} (Maximum)	oe -> pad	1.3	ns	50 pf load
Output, Medium	t_{PZX} (Maximum)	oe -> pad	4.8	ns	50 pf load
Output, Medium	t_{PXZ} (Maximum)	oe -> pad	1.9	ns	50 pf load
Output, Fast	t_{PZX} (Maximum)	oe -> pad	3.7	ns	50 pf load
Output, Fast	t_{PXZ} (Maximum)	oe -> pad	1.6	ns	50 pf load

AC Timing Characteristics – 3.3V Operation

Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C
Maximum delays are the average of t_{PDLH} and t_{PDHL}.

Clocks and Reset Input buffers are measured from a V_{IH} of 1.5V at the input pad to the internal V_{IH} of 50% of V_{CC}.
Maximum times for clock input buffers and internal drivers are measured for rising edge delays only.

Cell Function	Parameter	Path	Device	-1	Units	Notes
Global Clocks and Set/Reset						
GCLK Input Buffer	t_{PD} (Maximum)	pad -> clock	AT40K05AL	1.1	ns	Rising edge clock
		pad -> clock	AT40K10AL	1.2	ns	
		pad -> clock	AT40K20AL	1.2	ns	
		pad -> clock	AT40K40AL	1.4	ns	
FCLK Input Buffer	t_{PD} (Maximum)	pad -> clock	AT40K05AL	0.7	ns	Rising edge clock
		pad -> clock	AT40K10AL	0.8	ns	
		pad -> clock	AT40K20AL	0.8	ns	
		pad -> clock	AT40K40AL	0.8	ns	
Clock Column Driver	t_{PD} (Maximum)	clock -> colclk	AT40K05AL	0.8	ns	Rising edge clock
		clock -> colclk	AT40K10AL	0.9	ns	
		clock -> colclk	AT40K20AL	1.0	ns	
		clock -> colclk	AT40K40AL	1.1	ns	
Clock Sector Driver	t_{PD} (Maximum)	colclk -> secclk	AT40K05AL	0.5	ns	Rising edge clock
		colclk -> secclk	AT40K10AL	0.5	ns	
		colclk -> secclk	AT40K20AL	0.5	ns	
		colclk -> secclk	AT40K40AL	0.5	ns	
GSRN Input Buffer	t_{PD} (Maximum)	pad -> GSRN	AT40K05AL	3.0	ns	From any pad to Global Set/Reset network
		pad -> GSRN	AT40K10AL	3.7	ns	
		pad -> GSRN	AT40K20AL	4.3	ns	
		pad -> GSRN	AT40K40AL	5.6	ns	
Global Clock to Output	t_{PD} (Maximum)	clock pad -> out	AT40K05AL	8.3	ns	Rising edge clock
		clock pad -> out	AT40K10AL	8.4	ns	Fully loaded clock tree
		clock pad -> out	AT40K20AL	8.6	ns	Rising edge DFF
		clock pad -> out	AT40K40AL	8.8	ns	20 mA output buffer
						50 pf pin load
Fast Clock to Output	t_{PD} (Maximum)	clock pad -> out	AT40K05AL	7.9	ns	Rising edge clock
		clock pad -> out	AT40K10AL	8.0	ns	Fully loaded clock tree
		clock pad -> out	AT40K20AL	8.1	ns	Rising edge DFF
		clock pad -> out	AT40K40AL	8.3	ns	20 mA output buffer
						50 pf pin load

AC Timing Characteristics – 3.3V Operation

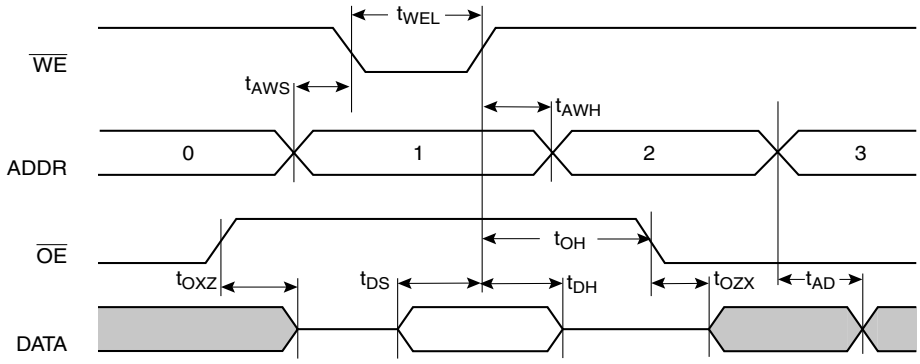
Delays are based on fixed loads and are described in the notes.
Maximum times based on worst case: V_{CC} = 3.0V, temperature = 70°C
Minimum times based on best case: V_{CC} = 3.6V, temperature = 0°C

Cell Function	Parameter	Path	-1	Units	Notes
Async RAM					
Write	t_{WECYC} (Minimum)	cycle time	12.0	ns	
Write	t_{WEL} (Minimum)	we	5.0	ns	Pulse width low
Write	t_{WEH} (Minimum)	we	5.0	ns	Pulse width high
Write	t_{AWS} (Minimum)	wr addr setup -> we	5.3	ns	
Write	t_{AWH} (Minimum)	wr addr hold -> we	0.0	ns	
Write	t_{DS} (Minimum)	din setup -> we	5.0	ns	
Write	t_{DH} (Minimum)	din hold -> we	0.0	ns	
Write/Read	t_{DD} (Maximum)	din -> dout	8.7	ns	rd addr = wr addr
Read	t_{AD} (Maximum)	rd addr -> dout	6.3	ns	
Read	t_{OZX} (Maximum)	oe -> dout	2.9	ns	
Read	t_{OXZ} (Maximum)	oe -> dout	3.5	ns	
Sync RAM					
Write	t_{CYC} (Minimum)	cycle time	12.0	ns	
Write	t_{CLKL} (Minimum)	clk	5.0	ns	Pulse width low
Write	t_{CLKH} (Minimum)	clk	5.0	ns	Pulse width high
Write	t_{WCS} (Minimum)	we setup -> clk	3.2	ns	
Write	t_{WCH} (Minimum)	we hold -> clk	0.0	ns	
Write	t_{ACS} (Minimum)	wr addr setup -> clk	5.0	ns	
Write	t_{ACH} (Minimum)	wr addr hold -> clk	0.0	ns	
Write	t_{DCS} (Minimum)	wr data setup -> clk	3.9	ns	
Write	t_{DCH} (Minimum)	wr data hold -> clk	0.0	ns	
Write/Read	t_{CD} (Maximum)	clk -> dout	5.8	ns	rd addr = wr addr
Read	t_{AD} (Maximum)	rd addr -> dout	6.3	ns	
Read	t_{OZX} (Maximum)	oe -> dout	2.9	ns	
Read	t_{OXZ} (Maximum)	oe -> dout	3.5	ns	

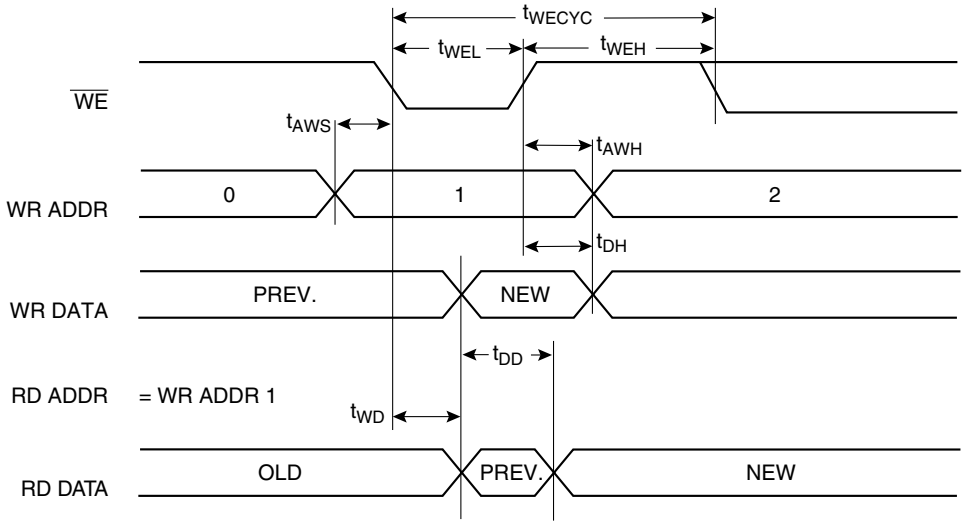
Notes:
1. CMOS buffer delays are measured from a V_{IH} of 1/2 V_{CC} at the pad to the internal V_{IH} at A. The input buffer load is constant.
2. Buffer delay is to a pad voltage of 1.5V with one output switching.
3. Parameter based on characterization and simulation; not tested in production.
4. Exact power calculation is available in Atmel FPGA Designer software.

FreeRAM Asynchronous Timing Characteristics

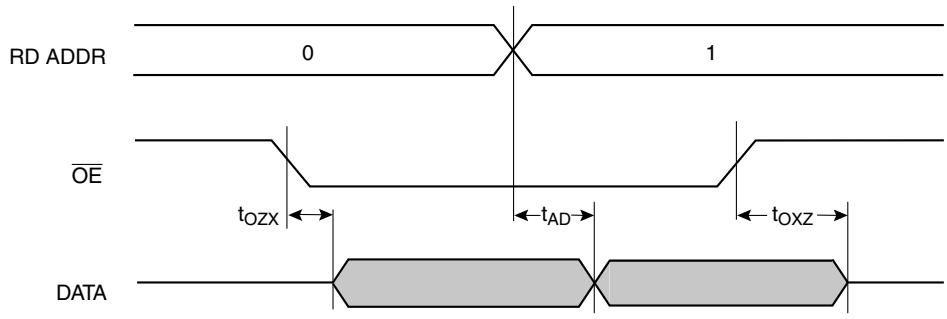
Single-port Write/Read



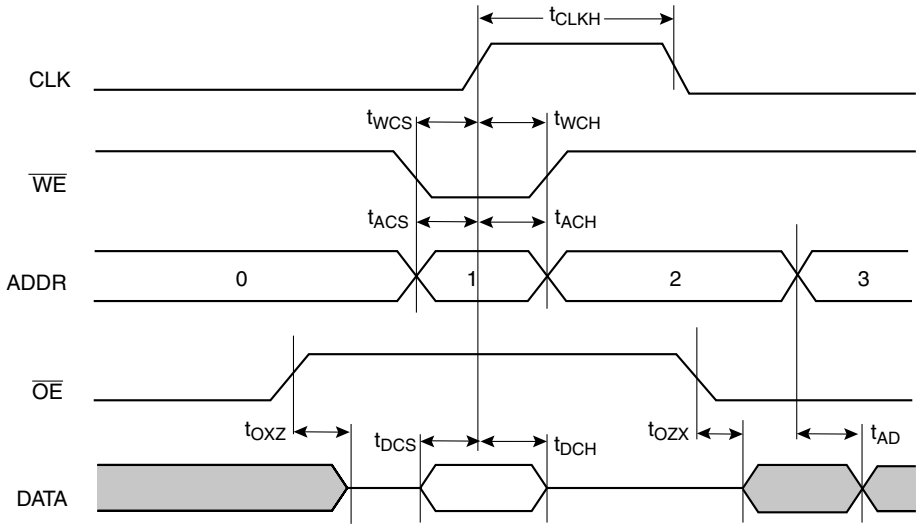
Dual-port Write with Read



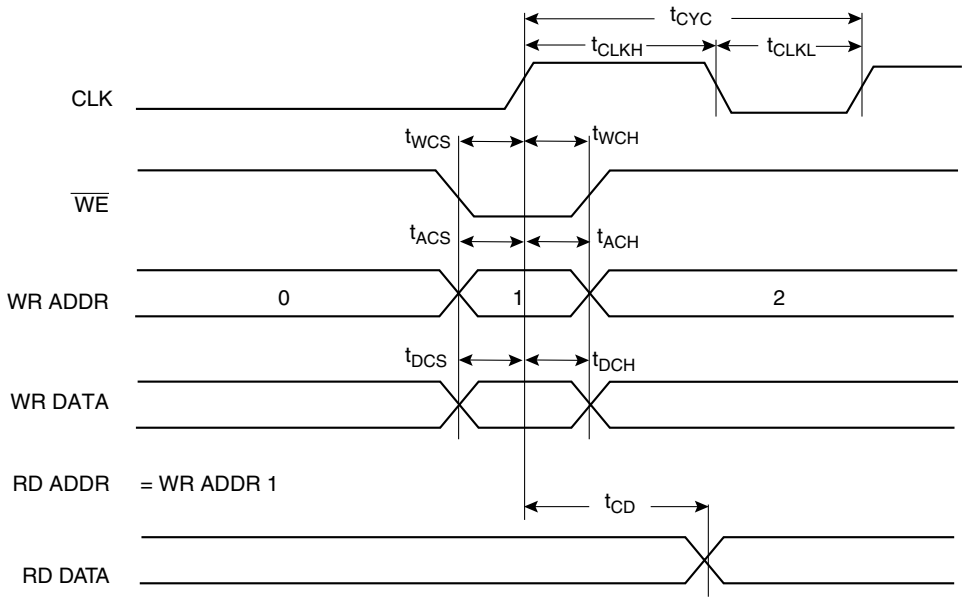
Dual-port Read



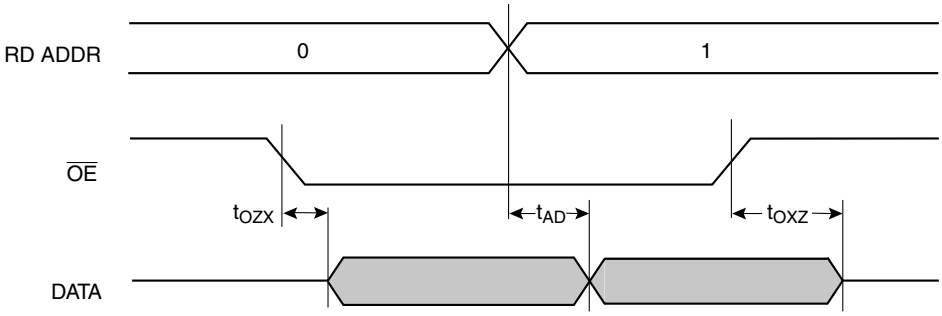
Single-port Write/Read



Dual-port Write with Read



Dual-port Read



AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)					
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP	352 SBGA[2]
GND	GND	GND	GND	12	1	1	2	1	GND[1]
I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	I/O1, GCK1 (A16)	13	2	2	4	2	D23
I/O2 (A17)	I/O2 (A17)	I/O2 (A17)	I/O2 (A17)	14	3	3	5	3	C25
I/O3	I/O3	I/O3	I/O3			4	6	4	D24
I/O4	I/O4	I/O4	I/O4			5	7	5	E23
I/O5 (A18)	I/O5 (A18)	I/O5 (A18)	I/O5 (A18)	15	4	6	8	6	C26
I/O6 (A19)	I/O6 (A19)	I/O6 (A19)	I/O6 (A19)	16	5	7	9	7	E24
			GND						
			I/O7						
			I/O8						
			I/O9						D25
			I/O10						F23
		I/O7	I/O11						F24
		I/O8	I/O12						E25
		VCC	VCC						VCC[1]
		GND	GND						GND[1]
			I/O13						
			I/O14						
I/O7	I/O7	I/O9	I/O15				10	8	D26
I/O8	I/O8	I/O10	I/O16				11	9	G24
	I/O9	I/O11	I/O17				12	10	F25
	I/O10	I/O12	I/O18				13	11	F26
			GND						
			I/O19						
			I/O20						
	I/O11	I/O13	I/O21					12	H23
	I/O12	I/O14	I/O22					13	H24
		I/O15	I/O23						G25
		I/O16	I/O24						G26

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. On-chip tri-state

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)					
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP	352 SBGA[2]
GND	GND	GND	GND			8	14	14	GND[1]
I/O9, FCK1	I/O13, FCK1	I/O17, FCK1	I/O25, FCK1			9	15	15	J23
I/O10	I/O14	I/O18	I/O26			10	16	16	J24
I/O11 (A20)	I/O15 (A20)	I/O19 (A20)	I/O27 (A20)	17	6	11	17	17	H25
I/O12 (A21)	I/O16 (A21)	I/O20 (A21)	I/O28 (A21)	18	7	12	18	18	K23
	VCC	VCC	VCC					19	VCC[1]
	I/O17	I/O21	I/O29					20	K24
	I/O18	I/O22	I/O30					21	J25
			GND						
			I/O31						
			I/O32						
			I/O33						J26
			I/O34						L23
		I/O23	I/O35						L24
		I/O24	I/O36						K25
		GND	GND					22	GND[1]
			VCC						VCC[1]
			I/O37						
			I/O38						
		I/O25	I/O39						L25
		I/O26	I/O40						L26
	I/O19	I/O27	I/O41				19	23	M23
	I/O20	I/O28	I/O42				20	24	M24
			GND						
I/O13	I/O21	I/O29	I/O43			13	21	25	M25
I/O14	I/O22	I/O30	I/O44		8	14	22	26	M26
			I/O45						
			I/O46						
I/O15 (A22)	I/O23 (A22)	I/O31 (A22)	I/O47 (A22)	19	9	15	23	27	N24

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. On-chip tri-state

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)					
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP	352 SBGA[2]
I/O16 (A23)	I/O24 (A23)	I/O32 (A23)	I/O48 (A23)	20	10	16	24	28	N25
GND	GND	GND	GND	21	11	17	25	29	GND[1]
VCC	VCC	VCC	VCC	22	12	18	26	30	VCC[1]
I/O17	I/O25	I/O33	I/O49	23	13	19	27	31	N26
I/O18	I/O26	I/O34	I/O50	24	14	20	28	32	P25
			I/O51						
			I/O52						
I/O19	I/O27	I/O35	I/O53		15	21	29	33	P23
I/O20	I/O28	I/O36	I/O54			22	30	34	P24
			GND						
	I/O29	I/O37	I/O55				31	35	R26
	I/O30	I/O38	I/O56				32	36	R25
		I/O39	I/O57						R24
		I/O40	I/O58						R23
			I/O59						
			I/O60						
			VCC						VCC
		GND	GND					37	GND[1]
		I/O41	I/O61						T26
		I/O42	I/O62						T25
			I/O63						
			I/O64						
			I/O65						T24
			I/O66						U25
			GND						
	I/O31	I/O43	I/O67					38	T23
	I/O32	I/O44	I/O68					39	V26
	VCC	VCC	VCC					40	VCC[1]
I/O21	I/O33	I/O45	I/O69	25	16	23	33	41	U24
I/O22	I/O34	I/O46	I/O70	26	17	24	34	42	V25
I/O23	I/O35	I/O47	I/O71			25	35	43	V24

Notes:
1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. On-chip tri-state

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)					
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP	352 SBGA[2]
I/O24, FCK2	I/O36, FCK2	I/O48, FCK2	I/O72, FCK2			26	36	44	U23
GND	GND	GND	GND			27	37	45	GND[1]
		I/O49	I/O73						Y26
		I/O50	I/O74						W25
	I/O37	I/O51	I/O75					46	W24
	I/O38	I/O52	I/O76					47	V23
			I/O77						
			I/O78						
			GND						
			I/O79						
			I/O80						
	I/O39	I/O53	I/O81				38	48	AA26
	I/O40	I/O54	I/O82				39	49	Y25
I/O25	I/O41	I/O55	I/O83				40	50	Y24
I/O26	I/O42	I/O56	I/O84				41	51	AA25
		GND	GND						GND[1]
		VCC	VCC						VCC[1]
		I/O57	I/O85						AB25
		I/O58	I/O86						AA24
			I/O87						
			I/O88						
I/O27	I/O43	I/O59	I/O89	27	18	28	42	52	Y23
I/O28	I/O44	I/O60	I/O90		19	29	43	53	AC26
			GND						
			I/O91						AD26
			I/O92						AC25
I/O29	I/O45	I/O61	I/O93			30	44	54	AA23
I/O30	I/O46	I/O62	I/O94			31	45	55	AB24
I/O31 ($\overline{OTS}$)[3]	I/O47 ($\overline{OTS}$)[3]	I/O63 ($\overline{OTS}$)[3]	I/O95 ($\overline{OTS}$)[3]	28	20	32	46	56	AD25
I/O32, GCK2	I/O48, GCK2	I/O64, GCK2	I/O96, GCK2	29	21	33	47	57	AC24

Notes:
1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. On-chip tri-state

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Left Side (Top to Bottom)					
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP	352 SBGA[2]
M1	M1	M1	M1	30	22	34	48	58	AB23
GND	GND	GND	GND	31	23	35	49	59	GND[1]
M0	M0	M0	M0	32	24	36	50	60	AD24

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. On-chip tri-state

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Bottom Side (Left to Right)					
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP	352 SBGA[2]
VCC	VCC	VCC	VCC	33	25	37	55	61	VCC[1]
M2	M2	M2	M2	34	26	38	56	62	AC23
I/O33, GCK3	I/O49, GCK3	I/O65, GCK3	I/O97, GCK3	35	27	39	57	63	AE24
I/O34 (HDC)	I/O50 (HDC)	I/O66 (HDC)	I/O98 (HDC)	36	28	40	58	64	AD23
I/O35	I/O51	I/O67	I/O99			41	59	65	AC22
I/O36	I/O52	I/O68	I/O100			42	60	66	AF24
I/O37	I/O53	I/O69	I/O101		29	43	61	67	AD22
I/O38 (LDC)	I/O54 (LDC)	I/O70 (LDC)	I/O102 (LDC)	37	30	44	62	68	AE23
			GND						
			I/O103						
			I/O104						
			I/O105						AC21
			I/O106						AD21
		I/O71	I/O107						AE22
		I/O72	I/O108						AF23
		VCC	VCC						VCC[1]
		GND	GND						GND[1]
I/O39	I/O55	I/O73	I/O109				63	69	AD20
I/O40	I/O56	I/O74	I/O110				64	70	AE21
	I/O57	I/O75	I/O111				65	71	AF21
	I/O58	I/O76	I/O112				66	72	AC19

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Bottom Side (Left to Right)					
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP	352 SBGA[2]
			I/O113						
			I/O114						
			GND						
		I/O77	I/O115						
		I/O78	I/O116						
	I/O59	I/O79	I/O117					73	AD19
	I/O60	I/O80	I/O118					74	AE20
			I/O119						AF20
			I/O120						AC18
GND	GND	GND	GND			45	67	75	GND[1]
I/O41	I/O61	I/O81	I/O121			46	68	76	AD18
I/O42	I/O62	I/O82	I/O122			47	69	77	AE19
I/O43	I/O63	I/O83	I/O123	38	31	48	70	78	AC17
I/O44	I/O64	I/O84	I/O124	39	32	49	71	79	AD17
	VCC	VCC	VCC					80	VCC[1]
	I/O65	I/O85	I/O125				72	81	AE18
	I/O66	I/O86	I/O126				73	82	AF18
			GND						
			I/O127						
			I/O128						
			I/O129						AC16
			I/O130						AD16
		I/O87	I/O131						AE17
		I/O88	I/O132						AE16
		GND	GND					83	GND[1]
			VCC						VCC[1]
		I/O89	I/O133						AF16
		I/O90	I/O134						AC15
	I/O67	I/O91	I/O135					84	AD15
	I/O68	I/O92	I/O136					85	AE15
I/O45	I/O69	I/O93	I/O137		33	50	74	86	AF15
I/O46	I/O70	I/O94	I/O138		34	51	75	87	AD14
			GND						

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Bottom Side (Left to Right)					
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP	352 SBGA[2]
			I/O139						
			I/O140						
			I/O141						
			I/O142						
I/O47 (D15)	I/O71 (D15)	I/O95 (D15)	I/O143 (D15)	40	35	52	76	88	AE14
I/O48 (INIT)	I/O72 (INIT)	I/O96 (INIT)	I/O144 (INIT)	41	36	53	77	89	AF14
VCC	VCC	VCC	VCC	42	37	54	78	90	VCC[1]
GND	GND	GND	GND	43	38	55	79	91	GND[1]
I/O49 (D14)	I/O73 (D14)	I/O97 (D14)	I/O145 (D14)	44	39	56	80	92	AE13
I/O50 (D13)	I/O74 (D13)	I/O98 (D13)	I/O146 (D13)	45	40	57	81	93	AC13
			I/O147						
			I/O148						
			I/O149						
			I/O150						
			GND						
I/O51	I/O75	I/O99	I/O151		41	58	82	94	AD13
I/O52	I/O76	I/O100	I/O152		42	59	83	95	AF12
	I/O77	I/O101	I/O153				84	96	AE12
	I/O78	I/O102	I/O154				85	97	AD12
		I/O103	I/O155						AC12
		I/O104	I/O156						AF11
			VCC						VCC[1]
		GND	GND					98	GND[1]
		I/O105	I/O157						AE11
		I/O106	I/O158						AD11
			I/O159						AE10
			I/O160						AC11
			I/O161						
			I/O162						
			GND						

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Bottom Side (Left to Right)					
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP	352 SBGA[2]
	I/O79	I/O107	I/O163					99	AF9
	I/O80	I/O108	I/O164					100	AD10
	VCC	VCC	VCC					101	VCC[1]
I/O53 (D12)	I/O81 (D12)	I/O109 (D12)	I/O165 (D12)	46	43	60	86	102	AE9
I/O54 (D11)	I/O82 (D11)	I/O110 (D11)	I/O166 (D11)	47	44	61	87	103	AD9
I/O55	I/O83	I/O111	I/O167			62	88	104	AC10
I/O56	I/O84	I/O112	I/O168			63	89	105	AF7
GND	GND	GND	GND			64	90	106	GND[1]
		I/O113	I/O169						AE8
		I/O114	I/O170						AD8
	I/O85	I/O115	I/O171					107	AC9
	I/O86	I/O116	I/O172					108	AF6
			I/O173						
			I/O174						
			GND						
			I/O175						
			I/O176						
	I/O87	I/O117	I/O177				91	109	AE7
	I/O88	I/O118	I/O178				92	110	AD7
I/O57	I/O89	I/O119	I/O179				93	111	AE6
I/O58	I/O90	I/O120	I/O180				94	112	AE5
		GND	GND						GND[1]
		VCC	VCC						VCC[1]
		I/O121	I/O181						AD6
		I/O122	I/O182						AC7
I/O59 (D10)	I/O91 (D10)	I/O123 (D10)	I/O183 (D10)	48	45	65	95	113	AF4
I/O60 (D9)	I/O92 (D9)	I/O124 (D9)	I/O184 (D9)	49	46	66	96	114	AF3
			I/O185						AE4
			I/O186						AC6
			GND						

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Bottom Side (Left to Right)					
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP	352 SBGA[2]
			I/O187						
			I/O188						
I/O61	I/O93	I/O125	I/O189			67	97	115	AD5
I/O62	I/O94	I/O126	I/O190			68	98	116	AE3
I/O63 (D8)	I/O95 (D8)	I/O127 (D8)	I/O191 (D8)	50	47	69	99	117	AD4
I/O64, GCK4	I/O96, GCK4	I/O128, GCK4	I/O192, GCK4	51	48	70	100	118	AC5
GND	GND	GND	GND	52	49	71	101	119	GND[1]
$\overline{CON}$	$\overline{CON}$	$\overline{CON}$	$\overline{CON}$	53	50	72	103	120	AD3

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Right Side (Bottom to Top)					
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP	352 SBGA[2]
VCC	VCC	VCC	VCC	54	51	73	106	121	VCC[1]
$\overline{RESET}$	$\overline{RESET}$	$\overline{RESET}$	$\overline{RESET}$	55	52	74	108	122	AC4
I/O65 (D7)	I/O97 (D7)	I/O129 (D7)	I/O193 (D7)	56	53	75	109	123	AD2
I/O66, GCK5	I/O98, GCK5	I/O130, GCK5	I/O194, GCK5	57	54	76	110	124	AC3
I/O67	I/O99	I/O131	I/O195			77	111	125	AB4
I/O68	I/O100	I/O132	I/O196			78	112	126	AD1
		I/O133	I/O197						AB3
		I/O134	I/O198						AC2
			GND						
	I/O101	I/O135	I/O199					127	AA4
	I/O102	I/O136	I/O200					128	AA3
			I/O201						
			I/O202						
			I/O203						AB2
			I/O204						AC1
		VCC	VCC						VCC[1]

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Right Side (Bottom to Top)					
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP	352 SBGA[2]
		GND	GND						GND[1]
I/O69 (D6)	I/O103 (D6)	I/O137 (D6)	I/O205 (D6)	58	55	79	113	129	Y3
I/O70	I/O104	I/O138	I/O206		56	80	114	130	AA2
I/O71	I/O105	I/O139	I/O207				115	131	AA1
I/O72	I/O106	I/O140	I/O208				116	132	W4
			I/O209						
			I/O210						
			GND						
			I/O211						
			I/O212						
	I/O107	I/O141	I/O213				117	133	W3
	I/O108	I/O142	I/O214				118	134	Y2
		I/O143	I/O215						Y1
		I/O144	I/O216						V4
GND	GND	GND	GND			81	119	135	GND[1]
	I/O109	I/O145	I/O217					136	V3
	I/O110	I/O146	I/O218					137	W2
I/O73, FCK3	I/O111, FCK3	I/O147, FCK3	I/O219, FCK3			82	120	138	U4
I/O74	I/O112	I/O148	I/O220			83	121	139	U3
	VCC	VCC	VCC					140	VCC[1]
I/O75 (D5)	I/O113 (D5)	I/O149 (D5)	I/O221 (D5)	59	57	84	122	141	V2
I/O76 (CS0)	I/O114 (CS0)	I/O150 (CS0)	I/O222 (CS0)	60	58	85	123	142	V1
			GND						
			I/O223						T4
			I/O224						T3
			I/O225						
			I/O226						
		I/O151	I/O227						U2
		I/O152	I/O228						T2
		GND	GND					143	GND[1]

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Right Side (Bottom to Top)					
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP	352 SBGA[2]
			VCC						VCC[1]
			I/O229						
			I/O230						
		I/O153	I/O231						T1
		I/O154	I/O232						R4
	I/O115	I/O155	I/O233				124	144	R3
	I/O116	I/O156	I/O234				125	145	R2
			GND						
I/O77	I/O117	I/O157	I/O235		59	86	126	146	R1
I/O78	I/O118	I/O158	I/O236		60	87	127	147	P3
			I/O237						
			I/O238						
I/O79(D4)	I/O119(D4)	I/O159(D4)	I/O239(D4)	61	61	88	128	148	P2
I/O80	I/O120	I/O160	I/O240	62	62	89	129	149	P1
VCC	VCC	VCC	VCC	63	63	90	130	150	VCC[1]
GND	GND	GND	GND	64	64	91	131	151	GND[1]
I/O81 (D3)	I/O121 (D3)	I/O161 (D3)	I/O241 (D3)	65	65	92	132	152	N2
I/O82 ($\overline{\text{CHECK}}$)	I/O122 ($\overline{\text{CHECK}}$)	I/O162 ($\overline{\text{CHECK}}$)	I/O242 ($\overline{\text{CHECK}}$)	66	66	93	133	153	N4
			I/O243						
			I/O244						
I/O83	I/O123	I/O163	I/O245		67	94	134	154	N3
I/O84	I/O124	I/O164	I/O246			95	135	155	M1
			GND						
	I/O125	I/O165	I/O247				136	156	M2
	I/O126	I/O166	I/O248				137	157	M3
		I/O167	I/O249						M4
		I/O168	I/O250						L1
			I/O251						
			I/O252						
			VCC						VCC[1]
		GND	GND					158	GND[1]

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Right Side (Bottom to Top)					
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP	352 SBGA[2]
		I/O169	I/O253						L2
		I/O170	I/O254						L3
			I/O255						K2
			I/O256						L4
			I/O257						
			I/O258						
			GND						
I/O85 (D2)	I/O127 (D2)	I/O171 (D2)	I/O259 (D2)	67	68	96	138	159	J1
I/O86	I/O128	I/O172	I/O260	68	69	97	139	160	K3
	VCC	VCC	VCC					161	VCC[1]
I/O87	I/O129	I/O173	I/O261			98	140	162	J2
I/O88, FCK4	I/O130, FCK4	I/O174, FCK4	I/O262, FCK4			99	141	163	J3
	I/O131	I/O175	I/O263					164	K4
	I/O132	I/O176	I/O264					165	G1
GND	GND	GND	GND			100	142	166	GND[1]
		I/O177	I/O265						H2
		I/O178	I/O266						H3
	I/O133	I/O179	I/O267					167	J4
	I/O134	I/O180	I/O268					168	F1
			I/O269						
			I/O270						
			GND						
	I/O135	I/O181	I/O271				143	169	G2
	I/O136	I/O182	I/O272				144	170	G3
I/O89	I/O137	I/O183	I/O273				145	171	F2
I/O90	I/O138	I/O184	I/O274				146	172	E2
			I/O275						
			I/O276						
		GND	GND						GND[1]
		VCC	VCC						VCC[1]
I/O91 (D1)	I/O139 (D1)	I/O185 (D1)	I/O277 (D1)	69	70	101	147	173	F3

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Right Side (Bottom to Top)					
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP	352 SBGA[2]
I/O92	I/O140	I/O186	I/O278	70	71	102	148	174	G4
			I/O279						D1
			I/O280						C1
			I/O281						
			I/O282						
			GND						
		I/O187	I/O283						D2
		I/O188	I/O284						F4
I/O93	I/O141	I/O189	I/O285			103	149	175	E3
I/O94	I/O142	I/O190	I/O286			104	150	176	C2
I/O95 (D0)	I/O143 (D0)	I/O191 (D0)	I/O287 (D0)	71	72	105	151	177	D3
I/O96, GCK6 ($\overline{CSOUT}$)	I/O144, GCK6 ($\overline{CSOUT}$)	I/O192, GCK6 ($\overline{CSOUT}$)	I/O288, GCK6 ($\overline{CSOUT}$)	72	73	106	152	178	E4
CCLK	CCLK	CCLK	CCLK	73	74	107	153	179	C3
VCC	VCC	VCC	VCC	74	75	108	154	180	VCC[1]
TSTCLK	TSTCLK	TSTCLK	TSTCLK	75	76	109	159	181	D4

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Top Side (Right to Left)					
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP	352 SBGA[2]
GND	GND	GND	GND	76	77	110	160	182	GND[1]
I/O97 (A0)	I/O145 (A0)	I/O193 (A0)	I/O289 (A0)	77	78	111	161	183	B3
I/O98, GCK7 (A1)	I/O146, GCK7 (A1)	I/O194, GCK7 (A1)	I/O290, GCK7 (A1)	78	79	112	162	184	C4
I/O99	I/O147	I/O195	I/O291			113	163	185	D5
I/O100	I/O148	I/O196	I/O292			114	164	186	A3
			I/O293						
			I/O294						

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. Shared with TSTCLK. No Connect.

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Top Side (Right to Left)					
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP	352 SBGA[2]
			GND						
			I/O295						C5
			I/O296						B4
I/O101 ($\overline{CS1}$,A2)	I/O149 ($\overline{CS1}$,A2)	I/O197 ($\overline{CS1}$,A2)	I/O297 ($\overline{CS1}$,A2)	79	80	115	165	187	D6
I/O102 (A3)	I/O150 (A3)	I/O198 (A3)	I/O298 (A3)	80	81	116	166	188	C6
		I/O199	I/O299						B5
		I/O200	I/O300						A4
		VCC	VCC						VCC[1]
		GND	GND						GND[1]
	I/O151[3]	I/O201[3]	I/O301[3]	75[3] NC	76[3] NC	109[3] NC	159[3] NC	189[3] NC	C7[3] NC
	I/O152	I/O202	I/O302					190	B6
I/O103	I/O153	I/O203	I/O303			117	167	191	A6
I/O104[3]	I/O154	I/O204	I/O304				168	192	D8
			I/O305						C8
			I/O306						
			GND						
			I/O307						
			I/O308						
	I/O155	I/O205	I/O309				169	193	B7
	I/O156	I/O206	I/O310				170	194	A7
		I/O207	I/O311					195	D9
		I/O208	I/O312						C9
GND	GND	GND	GND			118	171	196	GND[1]
I/O105	I/O157	I/O209	I/O313			119	172	197	B8
I/O106	I/O158	I/O210	I/O314			120	173	198	D10
	I/O159	I/O211	I/O315					199	C10
	I/O160	I/O212	I/O316					200	B9
	VCC	VCC	VCC					201	VCC[1]
		I/O213	I/O317						A9
		I/O214	I/O318						D11

Notes:
1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. Shared with TSTCLK. No Connect.

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Top Side (Right to Left)					
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP	352 SBGA[2]
			GND						
			I/O319						
			I/O320						
			I/O321						C11
			I/O322						B10
		I/O215	I/O323						B11
		I/O216	I/O324						A11
		GND	GND						GND[1]
			VCC						VCC[1]
I/O107 (A4)	I/O161 (A4)	I/O217 (A4)	I/O325 (A4)	81	82	121	174	202	D12
I/O108 (A5)	I/O162 (A5)	I/O218 (A5)	I/O326 (A5)	82	83	122	175	203	C12
	I/O163	I/O219	I/O327				176	205	B12
	I/O164	I/O220	I/O328				177	206	A12
I/O109	I/O165	I/O221	I/O329		84	123	178	207	C13
I/O110	I/O166	I/O222	I/O330		85	124	179	208	B13
			GND						
			I/O331						
			I/O332						
			I/O333						
			I/O334						
I/O111 (A6)	I/O167 (A6)	I/O223 (A6)	I/O335 (A6)	83	86	125	180	209	A13
I/O112 (A7)	I/O168 (A7)	I/O224 (A7)	I/O336 (A7)	84	87	126	181	210	B14
GND	GND	GND	GND	1	88	127	182	211	GND[1]
VCC	VCC	VCC	VCC	2	89	128	183	212	VCC[1]
I/O113 (A8)	I/O169 (A8)	I/O225 (A8)	I/O337 (A8)	3	90	129	184	213	D14
I/O114 (A9)	I/O170 (A9)	I/O226 (A9)	I/O338 (A9)	4	91	130	185	214	C14
			I/O339						
			I/O340						

Notes:
1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. Shared with TSTCLK. No Connect.

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Top Side (Right to Left)					
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP	352 SBGA[2]
			I/O341						
			I/O342						
			GND						
I/O115	I/O171	I/O227	I/O343		92	131	186	215	A15
I/O116	I/O172	I/O228	I/O344		93	132	187	216	B15
	I/O173	I/O229	I/O345				188	217	C15
	I/O174	I/O230	I/O346				189	218	D15
I/O117 (A10)	I/O175 (A10)	I/O231 (A10)	I/O347 (A10)	5	94	133	190	220	A16
I/O118 (A11)	I/O176 (A11)	I/O232 (A11)	I/O348 (A11)	6	95	134	191	221	B16
			VCC						VCC[1]
		GND	GND						GND[1]
		I/O233	I/O349						C16
		I/O234	I/O350						B17
			I/O351						D16
			I/O352						A18
			I/O353						
			I/O354						
			GND						
		I/O235	I/O355						C17
		I/O236	I/O356						B18
	VCC	VCC	VCC					222	VCC[1]
	I/O177	I/O237	I/O357					223	C18
	I/O178	I/O238	I/O358					224	D17
I/O119	I/O179	I/O239	I/O359			135	192	225	A20
I/O120	I/O180	I/O240	I/O360			136	193	226	B19
GND	GND	GND	GND			137	194	227	GND[1]
		I/O241	I/O361						C19
		I/O242	I/O362						D18
	I/O181	I/O243	I/O363				195	228	A21
	I/O182	I/O244	I/O364				196	229	B20
			I/O365						

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. Shared with TSTCLK. No Connect.

AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL	Top Side (Right to Left)					
128 I/O	192 I/O	256 I/O	384 I/O	84 PLCC	100 TQFP	144 LQFP	208 PQFP	240 PQFP	352 SBGA[2]
			I/O366						
			GND						
			I/O367						
			I/O368						
I/O121	I/O183	I/O245	I/O369				197	230	C20
I/O122	I/O184	I/O246	I/O370				198	231	B21
I/O123 (A12)	I/O185 (A12)	I/O247 (A12)	I/O371 (A12)	7	96	138	199	232	B22
I/O124 (A13)	I/O186 (A13)	I/O248 (A13)	I/O372 (A13)	8	97	139	200	233	C21
		GND	GND						GND[1]
		VCC	VCC						VCC[1]
		I/O249	I/O373						D20
		I/O250	I/O374						A23
			I/O375						A24
			I/O376						B23
			I/O377						
			I/O378						
			GND						
	I/O187	I/O251	I/O379					234	D21
	I/O188	I/O252	I/O380					235	C22
I/O125	I/O189	I/O253	I/O381			140	201	236	B24
I/O126	I/O190	I/O254	I/O382			141	202	237	C23
I/O127 (A14)	I/O191 (A14)	I/O255 (A14)	I/O383 (A14)	9	98	142	203	238	D22
I/O128, GCK8 (A15)	I/O192, GCK8 (A15)	I/O256, GCK8 (A15)	I/O384, GCK8 (A15)	10	99	143	204	239	C24
VCC	VCC	VCC	VCC	11	100	144	205	240	VCC[1]

Notes: 1. Pads labeled GND or VCC are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.
2. This package has an inverted die.
3. Shared with TSTCLK. No Connect.

Power and Ground Pinouts for 352 SBGA[1]

VCC Pins						
A10	A17	B2	B25	D7	D13	D19
G23	H4	K1	K26	N23	P4	U1
U26	W23	Y4	AC8	AC14	AC20	AE2
AE25	AF10	AF17				
GND Pins						
A1	A2	A5	A8	A14	A19	A22
A25	A26	B1	B26	E1	E26	H1
H26	N1	P26	W1	W26	AB1	AB26
AE1	AE26	AF1	AF2	AF5	AF8	AF13
AF19	AF22	AF25	AF26			

Note: 1. In SBGA packages, Power and Ground pins do not connect directly to die. They connect to Power and Ground planes inside the package.

Part/Package Availability and User I/O Counts (including Dual-function Pins)

Package[1]	AT40K05AL	AT40K10AL	AT40K20AL	AT40K40AL
84 PLCC	62	62	–	62
100 TQFP	78	78	78	–
144 LQFP	114	114	114	114
208 PQFP	128	161	161	161
240 PQFP	–	–	–	193
352 SBGA	–	–	–	289

Note: 1. Devices in same package are pin-to-pin compatible.

Package Type	
84J	84-lead, Plastic J-leaded Chip Carrier (PLCC)
100T1	100-lead, Thin (1.0 mm) Plastic Quad Flat Package (TQFP)
144L1	144-lead, Low-profile (1.4 mm) Plastic Quad Flat Package (LQFP)
208Q1	208-lead, Plastic Quad Flat Package (PQFP)
240Q1	240-lead, Plastic Quad Flat Package (PQFP)
352C1	252-ball, Enhanced, Low-profile Square Ball Grid Array Package (SBGA)

AT40K05AL Ordering Information

Usable Gates	Operating Voltage	Speed Grade (ns)	Ordering Code	Package	Operation Range[1]
5,000 - 10,000	3.3V	1	AT40K05AL-1AJC AT40K05AL-1AQC AT40K05AL-1BQC AT40K05AL-1DQC	84J 100T1 144L1 208Q1	Commercial (0°C to 70°C)
5,000 - 10,000	3.3V	1	AT40K05AL-1AJI AT40K05AL-1AQI AT40K05AL-1BQI AT40K05AL-1DQI	84J 100T1 144L1 208Q1	Industrial (-40°C to 85°C)

AT40K10AL Ordering Information

Usable Gates	Operating Voltage	Speed Grade (ns)	Ordering Code	Package	Operation Range[1]
10,000 - 20,000	3.3V	1	AT40K10AL-1AJC AT40K10AL-1AQC AT40K10AL-1BQC AT40K10AL-1DQC	84J 100T1 144L1 208Q1	Commercial (0°C to 70°C)
10,000 - 20,000	3.3V	1	AT40K10AL-1AJI AT40K10AL-1AQI AT40K10AL-1BQI AT40K10AL-1DQI	84J 100T1 144L1 208Q1	Industrial (-40°C to 85°C)

AT40K20AL Ordering Information

Usable Gates	Operating Voltage	Speed Grade (ns)	Ordering Code	Package	Operation Range[1]
20,000 - 30,000	3.3V	1	AT40K20AL-1AJC AT40K20AL-1AQC AT40K20AL-1BQC AT40K20AL-1DQC	84J 100T1 144L1 208Q1	Commercial (0°C to 70°C)
20,000 - 30,000	3.3V	1	AT40K20AL-1AJI AT40K20AL-1AQI AT40K20AL-1BQI AT40K20AL-1DQI	84J 100T1 144L1 208Q1	Industrial (-40°C to 85°C)

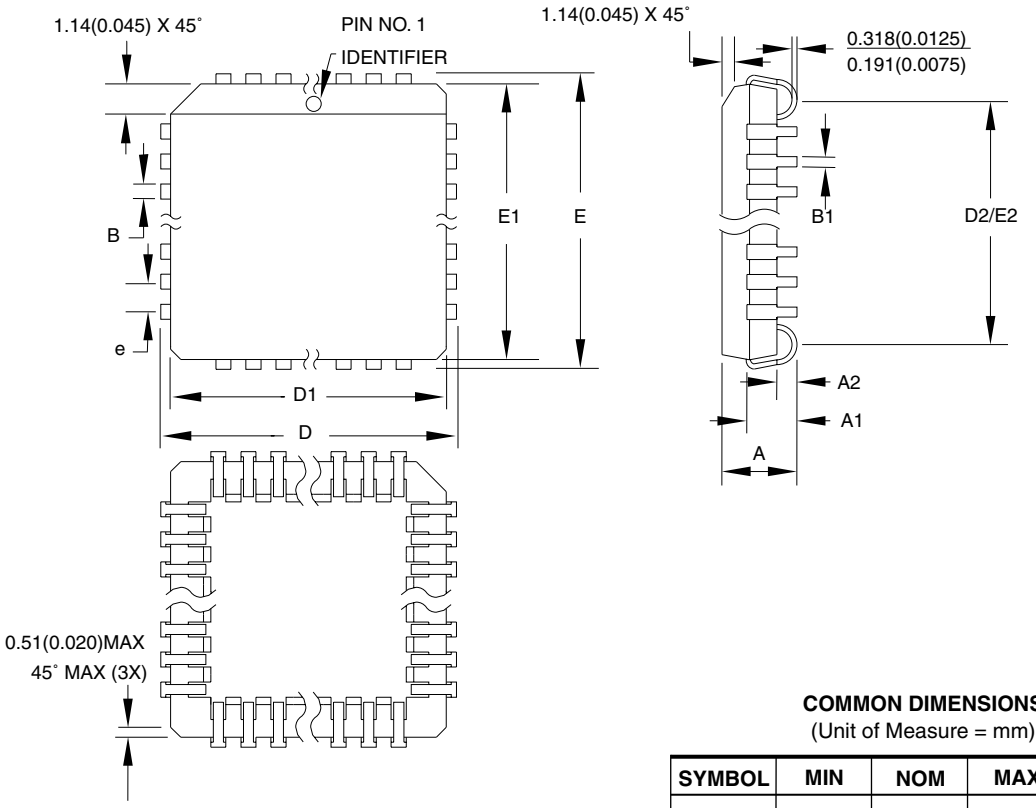
AT40K40AL Ordering Information

Usable Gates	Operating Voltage	Speed Grade (ns)	Ordering Code	Package	Operation Range[1]
40,000 - 50,000	3.3V	1	AT40K40AL-1BQC AT40K40AL-1DQC AT40K40AL-1EQC AT40K40AL-1BGC	144L1 208Q1 240Q1 352C1	Commercial (0°C to 70°C)
40,000 - 50,000	3.3V	1	AT40K40AL-1BQI AT40K40AL-1DQI AT40K40AL-1EQI AT40K40AL-1BGI	144L1 208Q1 240Q1 352C1	Industrial (-40°C to 85°C)

Note: 1. For military parts, contact Atmel at fpga@atmel.com.

Packaging Information

84J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

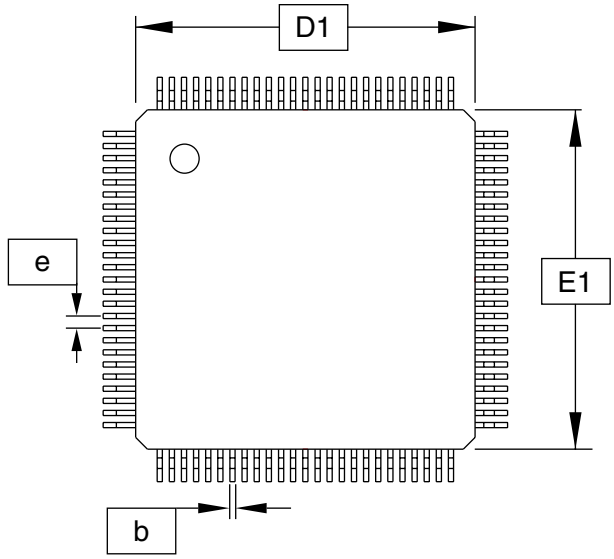
SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	30.099	–	30.353	
D1	29.210	–	29.413	Note 2
E	30.099	–	30.353	
E1	29.210	–	29.413	Note 2
D2/E2	27.686	–	28.702	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AF.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

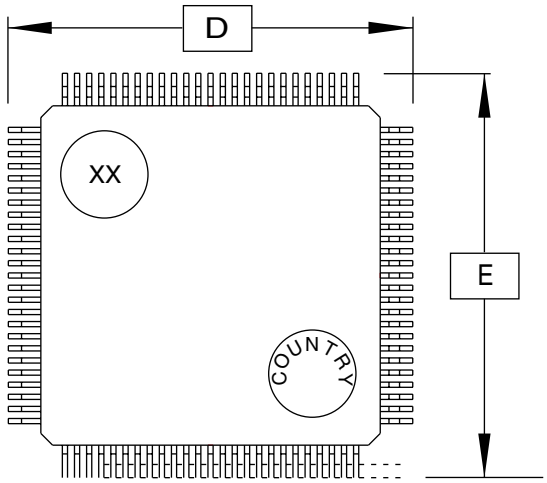
10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**84J**, 84-lead, Plastic J-leaded Chip Carrier (PLCC)	84J	B

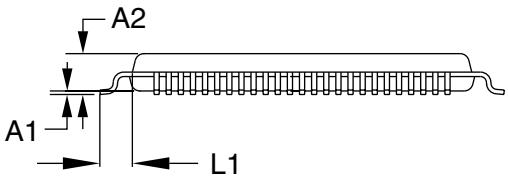
100T1 – TQFP



Top View



Bottom View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

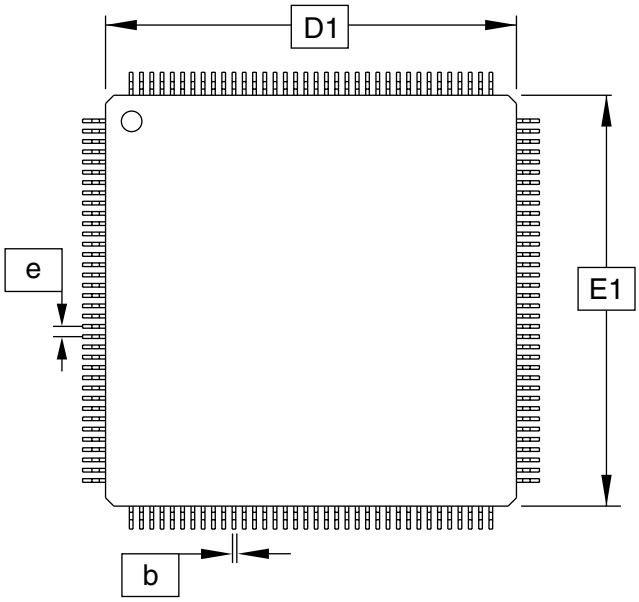
SYMBOL	MIN	NOM	MAX	NOTE
A1	0.05		0.15	6
A2	0.95	1.00	1.05	
D		16.00 BSC		
D1		14.00 BSC		2, 3
E		16.00 BSC		
E1		14.00 BSC		2, 3
e		0.50 BSC		
b	0.17	0.22	0.27	4, 5
L1		1.00 REF		

Notes: 1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions, including mold mismatch.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 and 0.5 mm pitch packages.
5. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
6. A1 is defined as the distance from the seating place to the lowest point on the package body.

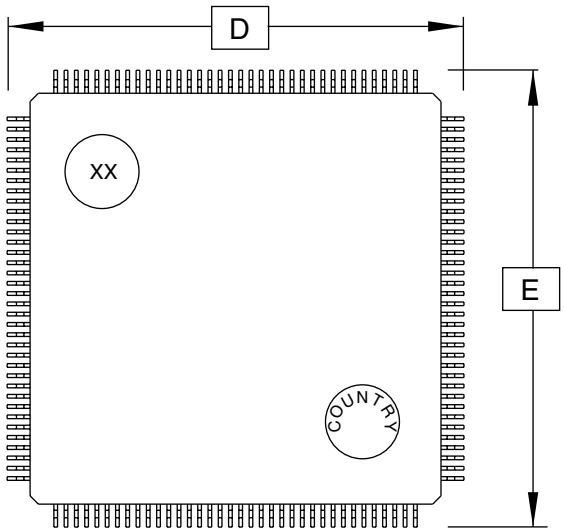
11/30/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**100T1**, 100-lead (14 x 14 x 1.0 mm Body), Thin Plastic Quad Flat Pack (TQFP)	100T1	A

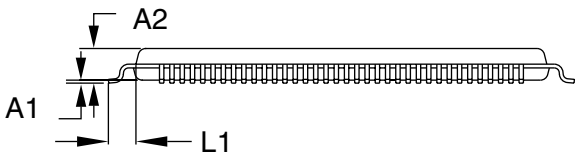
144L1 – LQFP



Top View



Bottom View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

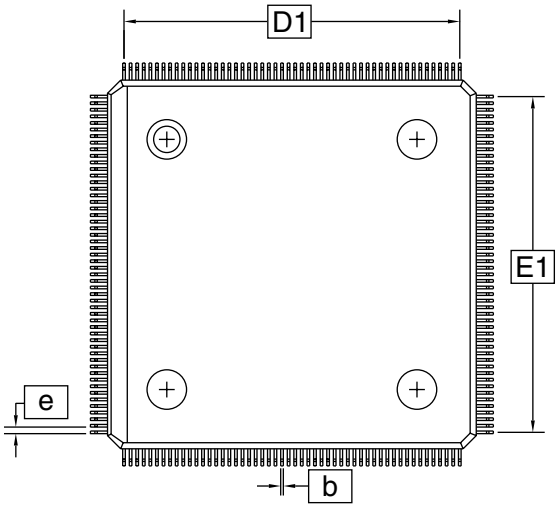
SYMBOL	MIN	NOM	MAX	NOTE
A1	0.05		0.15	6
A2	1.35	1.40	1.45	
D	22.00 BSC			
D1	20.00 BSC			2, 3
E	22.00 BSC			
E1	20.00 BSC			2, 3
e	0.50 BSC			
b	0.17	0.22	0.27	4, 5
L1	1.00 REF			

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-026 for additional information.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 and 0.5 mm pitch packages.
5. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
6. A1 is defined as the distance from the seating place to the lowest point on the package body.

11/30/01

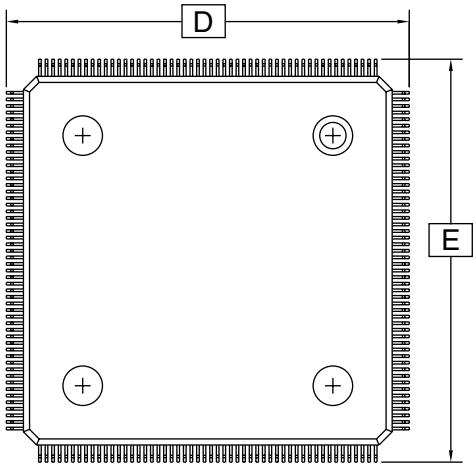
	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**144L1**, 144-lead (20 x 20 x 1.4 mm Body), Low Profile Plastic Quad Flat Pack (LQFP)	144L1	A

208Q1 – PQFP



Top View

Side View



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

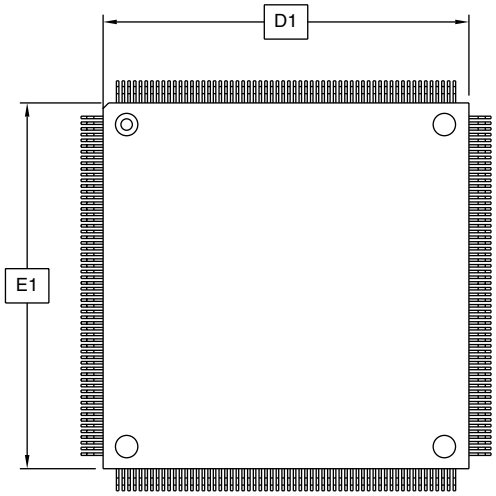
SYMBOL	MIN	NOM	MAX	NOTE
A1	0.25	–	0.50	
A2	3.20	3.40	3.60	
D		30.60 BSC		
D1		28.00 BSC		2, 3
E		30.60 BSC		
E1		28.00 BSC		2, 3
e		0.50 BSC		
b	0.17	–	0.27	4
L1		1.30 REF		

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-129, Variation FA-1, for proper dimensions, tolerances, datums, etc.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.

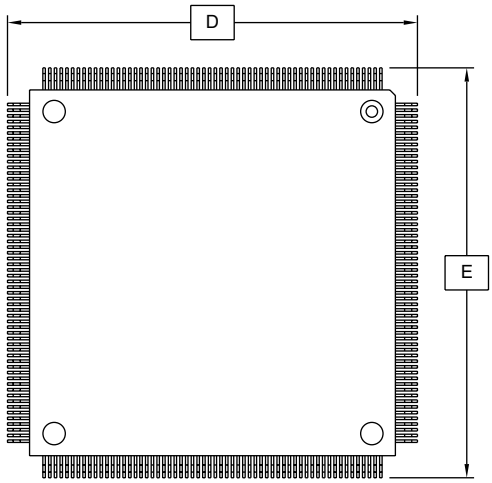
07/23/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**208Q1**, 208-lead (28 x 28 mm Body, 2.6 Form Opt.), Plastic Quad Flat Pack (PQFP)	208Q1	B

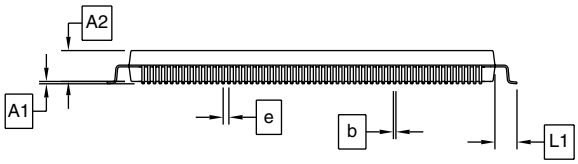
240Q1 – PQFP



Top View



Bottom View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

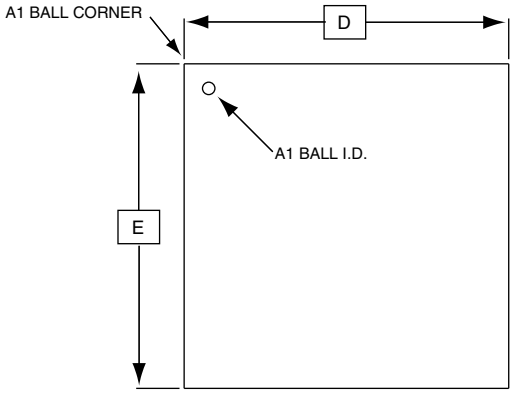
SYMBOL	MIN	NOM	MAX	NOTE
A1	0.25	–	0.50	
A2	3.20	3.40	3.60	
D		34.60 BSC		3
D1		32.00 BSC		2, 4
E		34.60 BSC		3
E1		32.00 BSC		2, 4
e		0.50 BSC		
b	0.17	–	0.27	5
L1		1.30 REF		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MS-029, Variation GA, for additional information.
2. All dimensioning and tolerancing conforms to ASME Y14.5M-1994.
3. To be determined at seating plane.
4. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch. Dimensions D1 and E1 shall be determined at datum plane.
5. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. The minimum space between protrusion and an adjacent lead shall not be less than 0.07 mm.

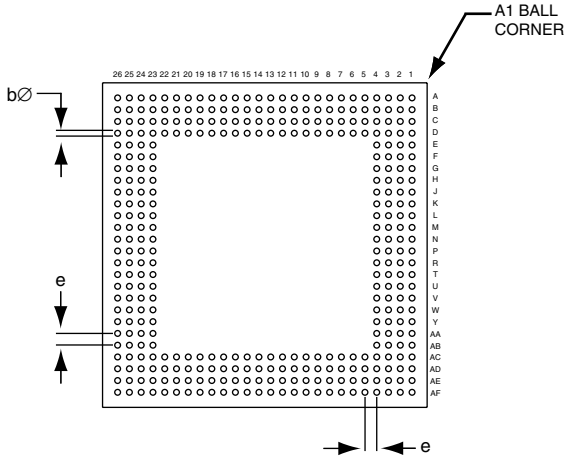
3/29/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**240Q1,** 240-lead, 32 x 32 mm Body, 2.6 Form Opt., Plastic Quad Flat Pack (PQFP)	240Q1	A

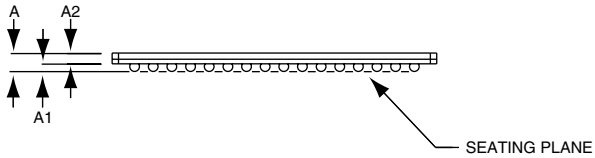
352C1 – SBGA



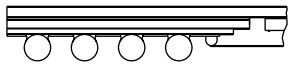
Top View



Bottom View
Die Side



Side View



Section View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D		35.0 BSC		
E		35.0 BSC		
Matrix Size		26 x 26		
A	–	–	1.70	
A1	0.35	–	–	
A2	0.25	–	1.10	
bØ	0.60	0.75	0.90	
e		1.27 BSC		

Notes: 1. This drawing is for general information only. Refer to JEDEC Drawing MO-192, Variation BAR-2, for additional information.
2. JEDEC variations are based on fully populated ball arrays. Arrays can be depopulated as desired by removing balls from the fully populated array.

3/29/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**352C1,** 352-ball, 35 x 35, Enhanced, Low-profile Square Ball Grid Array Package (SBGA)	352C1	A

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